User Guide for

FEBFAN9611_S01U300A
Evaluation Board

FAN9611 300W Interleaved Dual-BCM, Low-Profile, PFC Evaluation Board

Featured Fairchild Product:

FAN9611

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The following user guide supports the FAN9611 300W evaluation board for interleaved boundary-conduction-mode power-factor-corrected supply. It should be used in conjunction with the FAN9611 datasheet, Fairchild application note *AN-6086 —Design Considerations for Interleaved Boundary-Conduction Mode PFC Using FAN9611 / FAN9612* and FAN9611/12 PFC Excel®-based Design Tool.

1. Overview of the Evaluation Board

The FAN9611 interleaved, dual Boundary-Conduction-Mode (BCM), Power-Factor-Correction (PFC) controllers operate two parallel-connected boost power trains 180º out of phase. Interleaving extends the maximum practical power level of the control technique from about 300W to greater than 800W. Unlike the Continuous Conduction Mode (CCM) technique often used at higher power levels, BCM offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less expensive diodes without sacrificing efficiency. Furthermore, the input and output filters can be smaller due to ripple current cancellation between the power trains and doubling of effective switching frequency.

The advanced line feed-forward with peak detection circuit minimizes the output voltage variation during line transients. To guarantee stable operation with less switching loss at light load, the maximum switching frequency is clamped at 525kHz. Synchronization is maintained under all operating conditions.

Protection functions include output over-voltage, over-current, open-feedback, under-voltage lockout, brownout, and redundant latching over-voltage protection. FAN9611 is available in a lead-free, 16-lead, Small-Outline Integrated-Circuit (SOIC) package.

This FAN9611 evaluation board uses a four-layer Printed Circuit Board (PCB) designed for 300W (400V/0.75A) rated power. The maximum rated power is 350W and the Maximum On-Time (MOT) power limit is set to 360W. The FEBFAN9611_S01U300A is optimized to demonstrate all the FAN9611 efficiency and protection features in a low-profile height form factor less than 18mm.

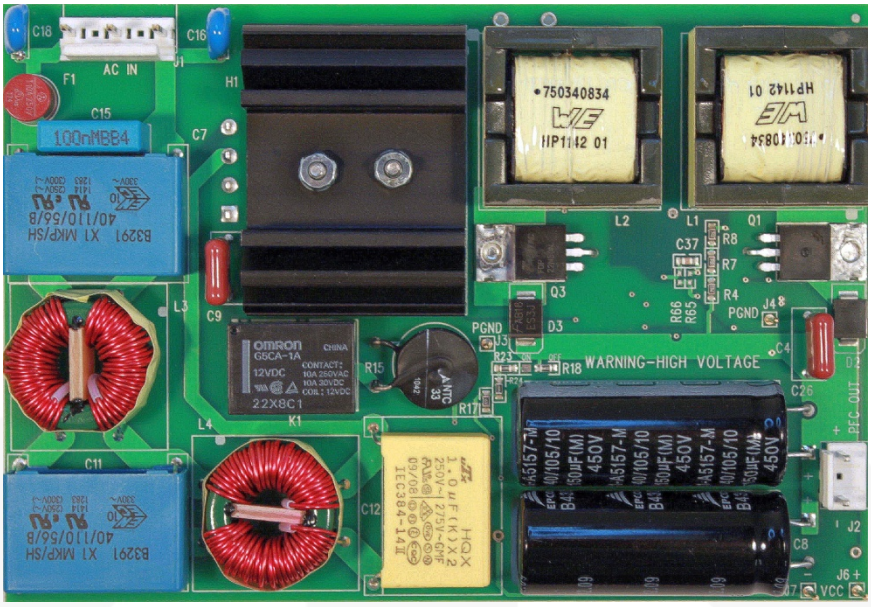


Figure 1. FEBFAN9611_S01U300A, Top View, 152mm x 105mm

Figure 2. FEBFAN9611_S01U300A, Side View (Low Profile), Cross Section=18mm

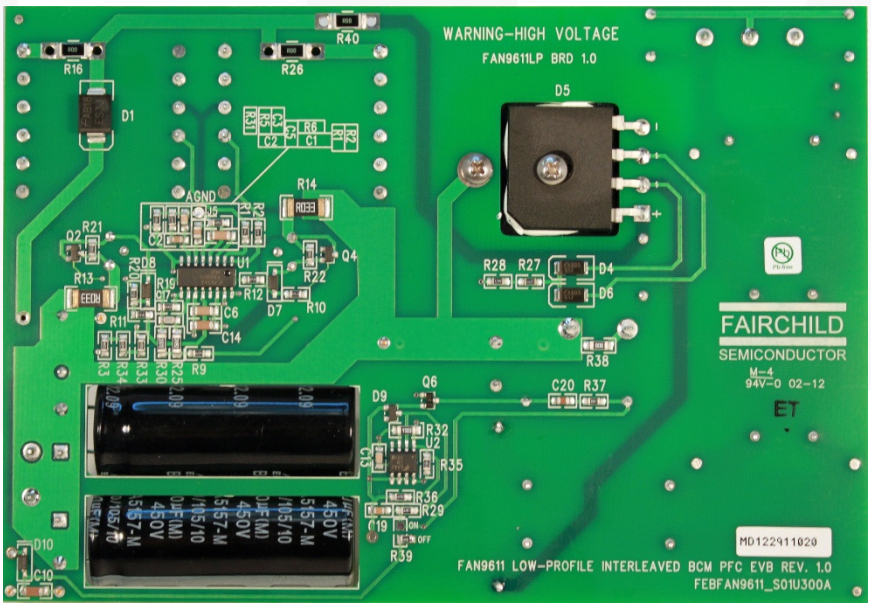


Figure 3. FEBFAN9611_S01U300A, Bottom View, 152mm x 105mm

2. Key Features

- 180° Out-of-Phase Synchronization
- Automatic Phase Disable at Light Load
- 1.8A Sink, 1.0A Source, High-Current Gate Drivers
- Transconductance (g_M) Error Amplifier for Reduced Overshoot
- Voltage-Mode Control with $(V_{IN})^2$ Feed-Forward
- Closed-Loop Soft-Start with Programmable Soft-Start Time for Reduced Overshoot
- Minimum Restart Timer Frequency to Avoid Audible Noise
- Maximum Switching Frequency Clamp
- Brownout Protection with Soft Recovery
- Non-Latching OVP on FB Pin and Second-Level Latching Protection on OVP Pin
- Open-Feedback Protection
- Over-Current and Power-Limit Protection for Each Phase
- Low Startup Current: 80µA Typical
- Works with DC input or 50Hz to 400Hz AC Input

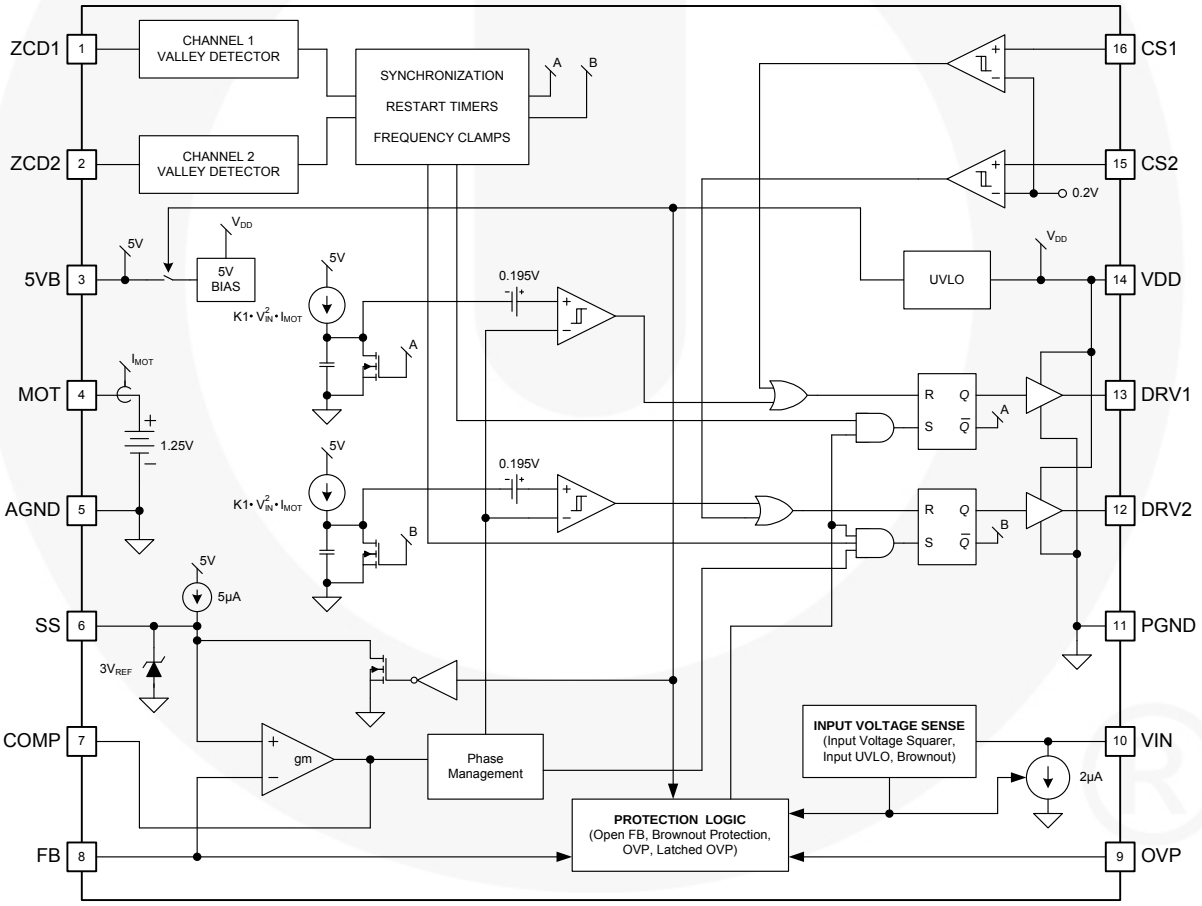


Figure 4. Block Diagram

3. Specifications

This evaluation board has been designed and optimized for the conditions in Table 1.

Table 1. Electrical and Mechanical Requirements

	Min.	Typ.	Max.
V_{IN_AC}	80V	120V	265V
$V_{IN\_AC(ON)}$		90V	
$V_{IN\_AC(OFF)}$		80V	
f_{VIN_AC}	50Hz	60Hz	65Hz
V_{OUT_PFC}	395V	400V	405V
$V_{OUT\_PFC\_RIPPLE}$		10V	11V
P_{OUT_PFC}		300W	350W
$P_{OUT\_PFC(MOT\ LIMIT)}$		360W	
f_{SW_PFC}	18kHz		300kHz
t_{HOLD_UP}	20ms		
t_{SOFT_START}		250ms	300ms
$t_{ON\_OVERSHOOT}$			10V
$\eta_{\_PFC\_120V}$ P_{OUT}>30%$P_{OUT(TYP)}$		96%	96.5%
$\eta_{\_PFC\_230V}$ P_{OUT}>30%$P_{OUT(TYP)}$		95%	98%
$PF_{\_120V}$			0.991
$PF_{\_230V}$			0.980
Mechanical and Thermal			
Height			18mm
θ_{JC}			60^{0}C

The trip points for the built-in protections are set as below in the evaluation board.

- The line UVLO (brownout protection) trip point is set at 80V_{AC} (10V_{AC} hysteresis).
- The pulse-by-pulse current limit for each MOSFET is set at 6A.

The current-limit function can be observed by measuring the individual inductor current waveforms while operating at 85V_{AC} and increasing the load to 360W. The maximum power limit is set at ~120% of the rated output power. The power-limit function can be observed while operating at >115V_{AC} and increasing the load beyond 360W. When operating in power limit, the output voltage drops and the COMP voltage is saturated, but the AC line current remains sinusoidal. The phase-management function permits phase shedding / adding ~18% of the nominal output power for high line (230V_{AC}). This level can be increased by modifying the MOT resistor (R6) as described in Fairchild Application Note *AN-6086 —Design Considerations for Interleaved Boundary-Conduction Mode PFC Using FAN9611 / FAN9612*.

4. Test Procedure

Before applying power to the FEBFAN9611_S01U300A evaluation board; the DC bias supply for V_{DD}, AC voltage supply for line input, and DC electronic load for output should be connected to the board as shown in Figure 5.

Table 2. Specification Excerpt from FAN9611 Datasheet

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
$I_{STARTUP}$	Startup Supply Current	$V_{DD} = V_{ON} – 0.2V$		80	110	µA
I_{DD}	Operating Current	Output Not Switching		3.7	5.2	mA
I_{DD_DYM}	Dynamic Operating Current	f_{SW} = 50kHz; C_{LOAD} = 2nF		4	6	mA
V_{ON}	UVLO Start Threshold	V_{DD} Increasing	9.5	10.0	10.5	V
V_{OFF}	UVLO Stop Threshold Voltage	V_{DD} Decreasing	7.0	7.5	8.0	V
V_{HYS}	UVLO Hysteresis	$V_{ON} – V_{OFF}$		2.5		V

4.1. Safety Precautions

The FEBFAN9611_S01U300A evaluation module produces lethal voltages and the bulk output capacitors store significant charge. Please be extra careful when probing and handling the module and observe a few precautions:

- Start with a clean working surface, clear of any conductive material.
- Be careful while turning on the power switch to the AC source.
- Never probe or move a probe on the DUT while the AC line voltage is present.
- Ensure the output capacitors are discharged before disconnecting the test leads. One way to do this is to remove the AC power with the DC output load still switched on. The load then discharges the output capacitors and the module is safe to disconnect.

Power-On Procedure

1. Supply V_{DD} for the control chip first. It should be higher than 10.5V *(refer to the specification for V_{DD} turn-on threshold voltage in Table 2).*
2. Connect the AC voltage (90~265V_{AC}) to start the FAN9611 evaluation board. Since FAN9611 has brownout protection, any input voltage less than the designed minimum AC line voltage triggers brownout protection. FEBFAN9611_S01U300A does not start until the AC input voltage is greater than 90V_{AC}.
3. Change load current (0~0.75A) and check the operation
4. Verify the output voltage is regulating between 395V_{DC}<V_{OUT}<405V_{DC}

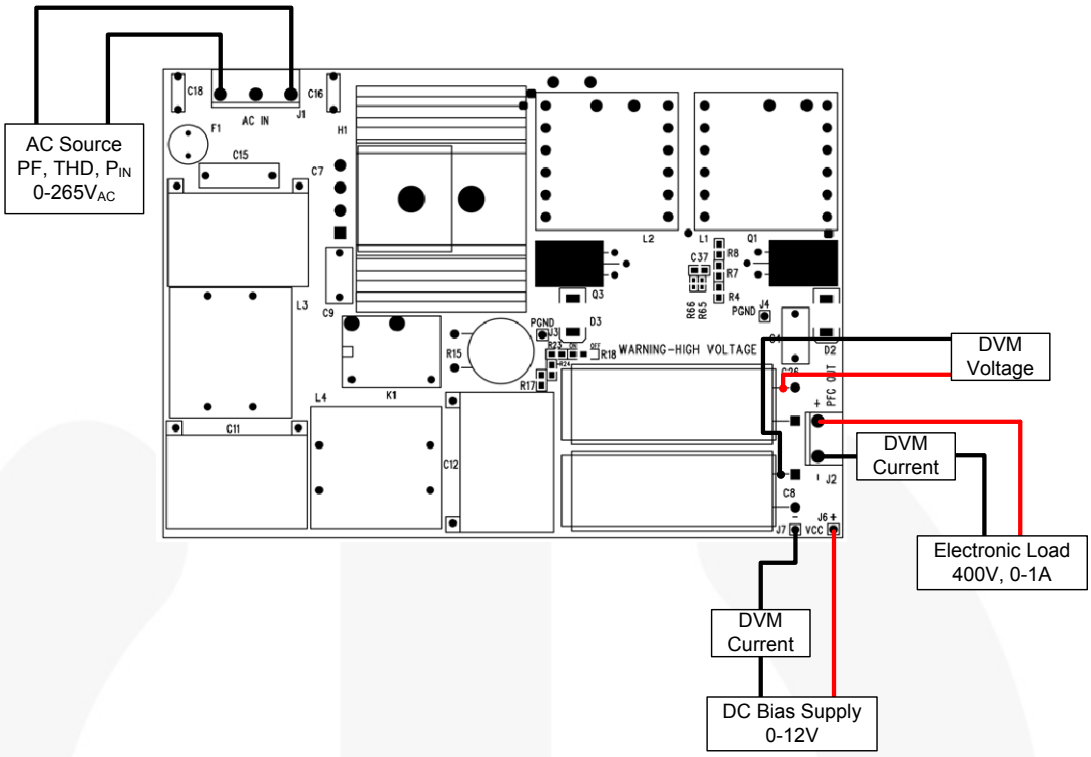


Figure 5. Recommended Test Set-Up

All efficiency data shown in this document was taken using the test set up shown in Figure 5 with the output voltage being measured directly at the output bulk capacitors (not through the output connector (J2)).

Power-Off Procedure

1. Make sure the electronic load is set to draw at least 100mA of constant DC current.
2. Disconnect (shut down) AC line voltage source.
3. Disconnect (shut down) 12V DC bias power supply.
4. Disconnect (shut down) DC electronic load last to ensure that the output capacitors are fully discharged before handling the evaluation module.

5. Schematic

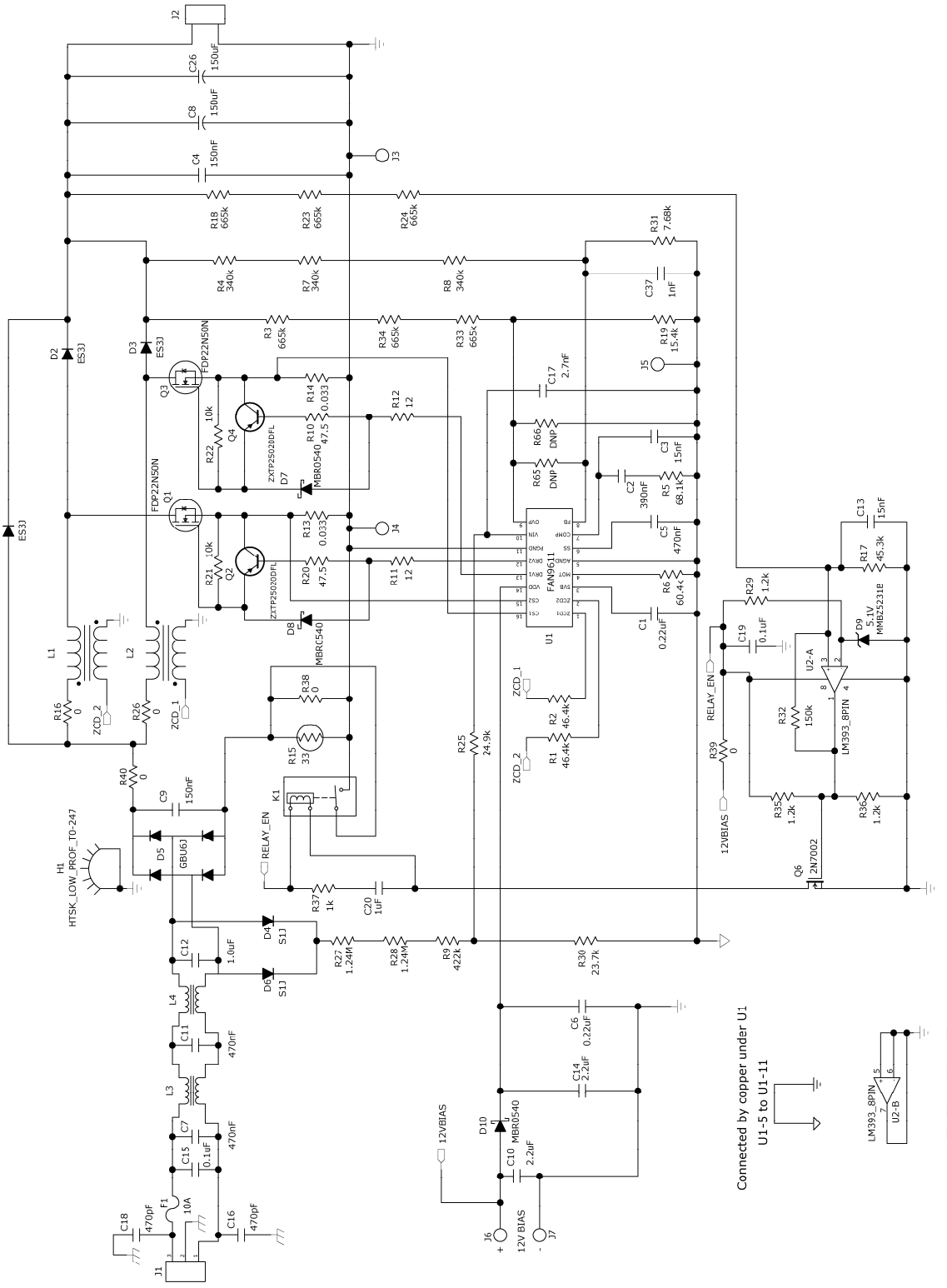


Figure 6. FEBFAN9611_S01U300A 300W Evaluation Board Schematic

6. Boost Inductor Specification

750340834 from Wurth Electronics (www.we-online.com)

- Core: EFD30 (A_e=69mm^2)
- Bobbin: EFD30
- Inductance : 270µH

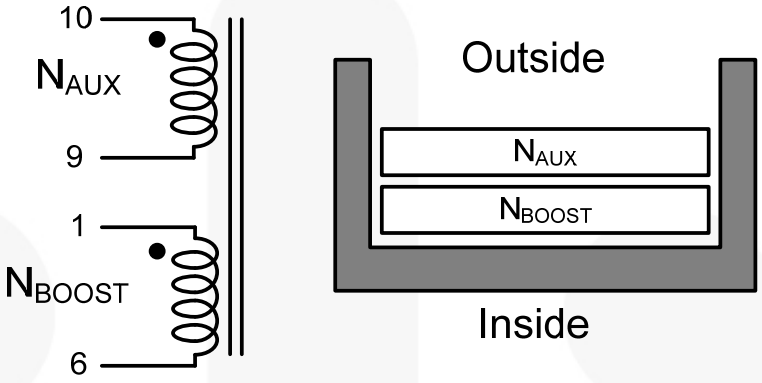


Figure 7. Boost Inductor (L1, L2) in the Evaluation Board

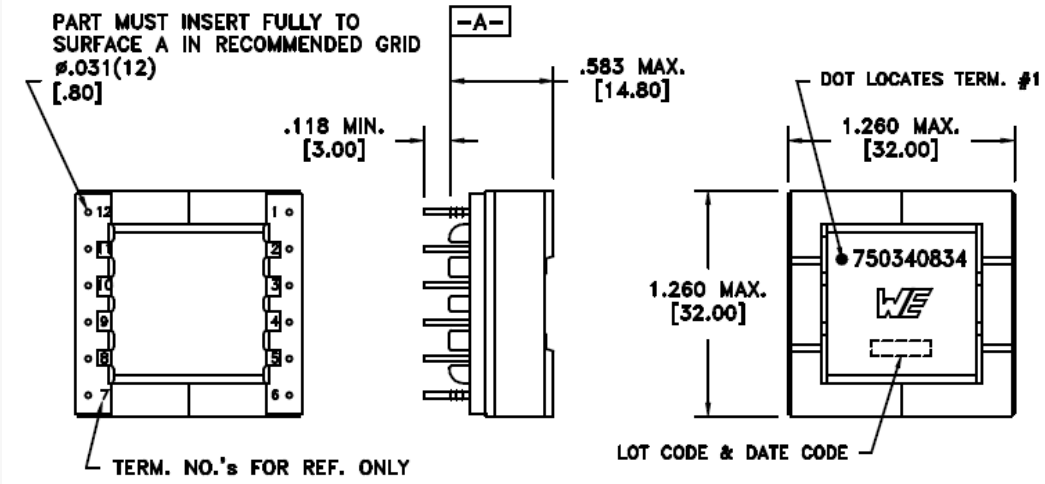


Figure 8. Wurth 750340834 Mechanical Drawing

Table 3. Inductor Turns Specifications

	Pin	Turns	Wire
N_{BOOST}	1 → 6	69 (3 Layers)	30xAWG#38 Litz
Insulation Tape			
N_{AUX}	10 → 9	7	AWG#28
Insulation Tape			

7. Four-Layer PCB and Assembly Images

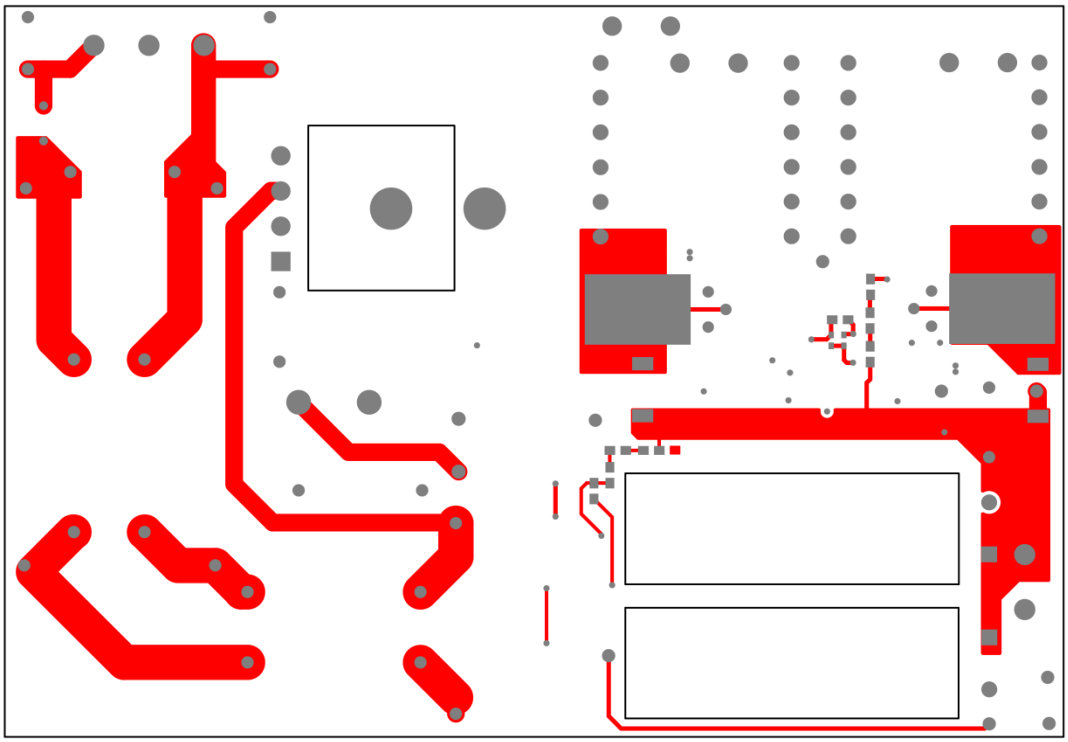


Figure 9. Layer 1 – Top Layer

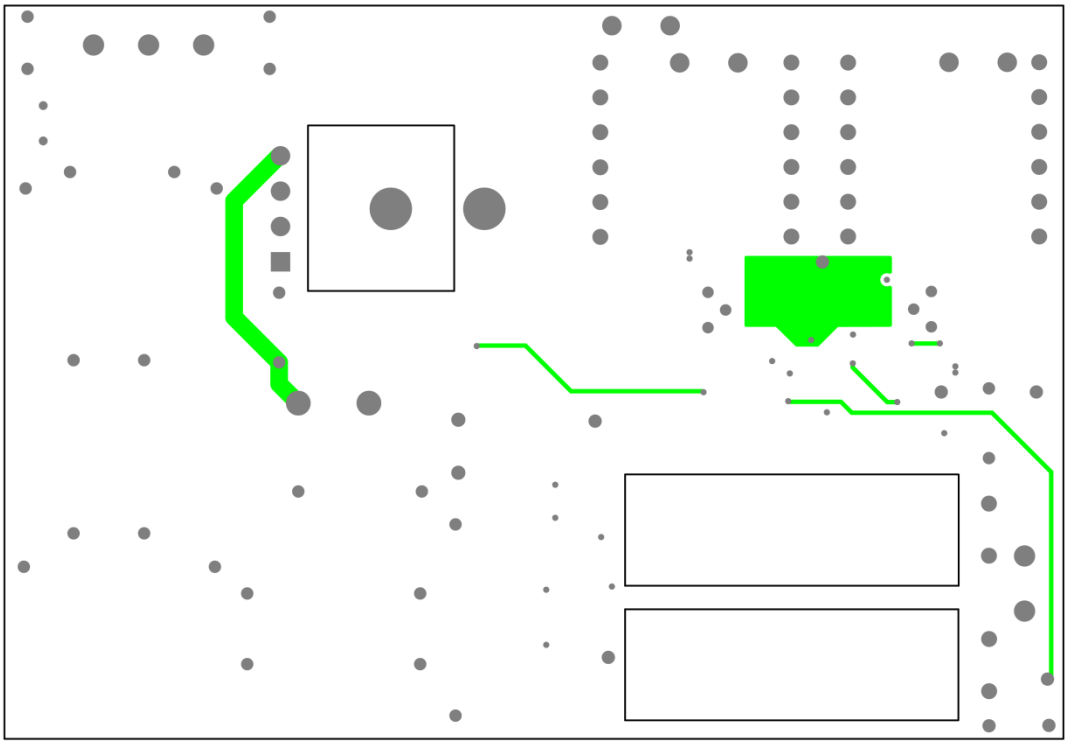


Figure 10. Layer 2 – Internal Layer

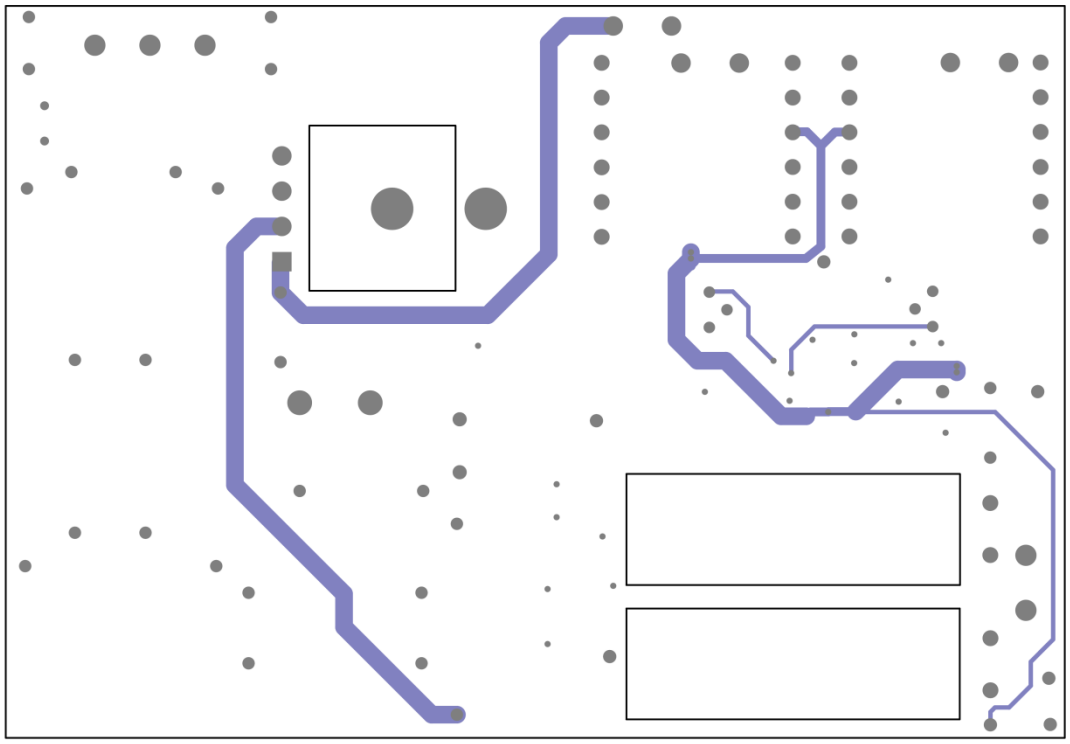


Figure 11. Layer 3 – Internal Layer

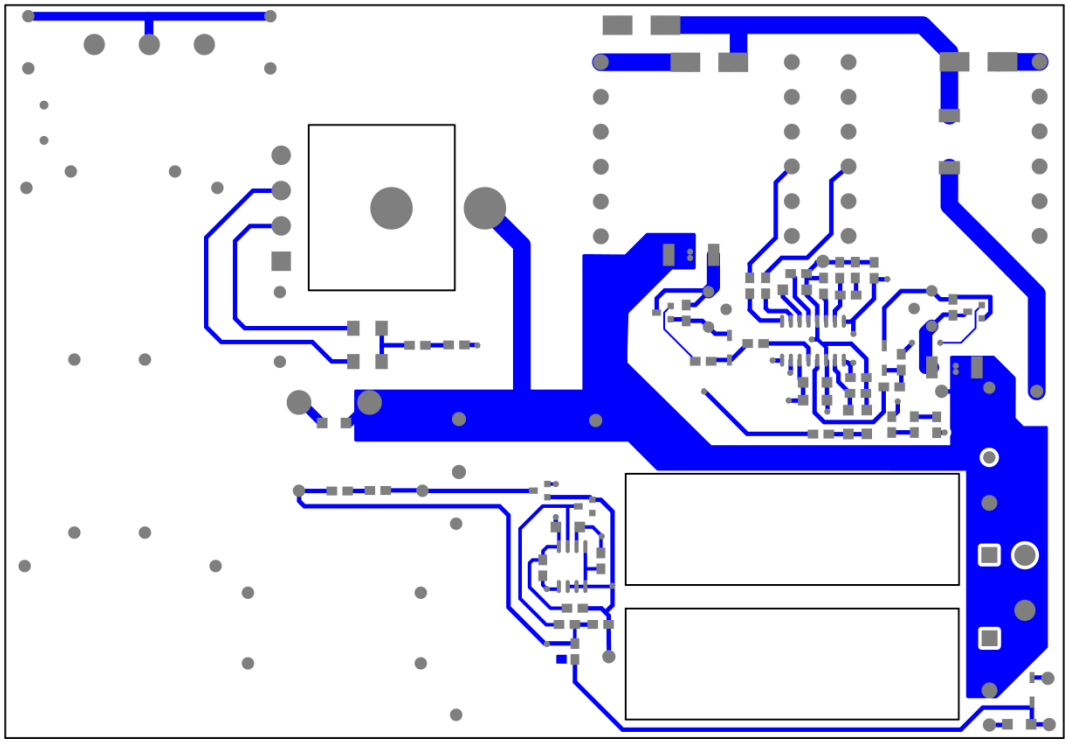


Figure 12. Layer 4 – Bottom Layer

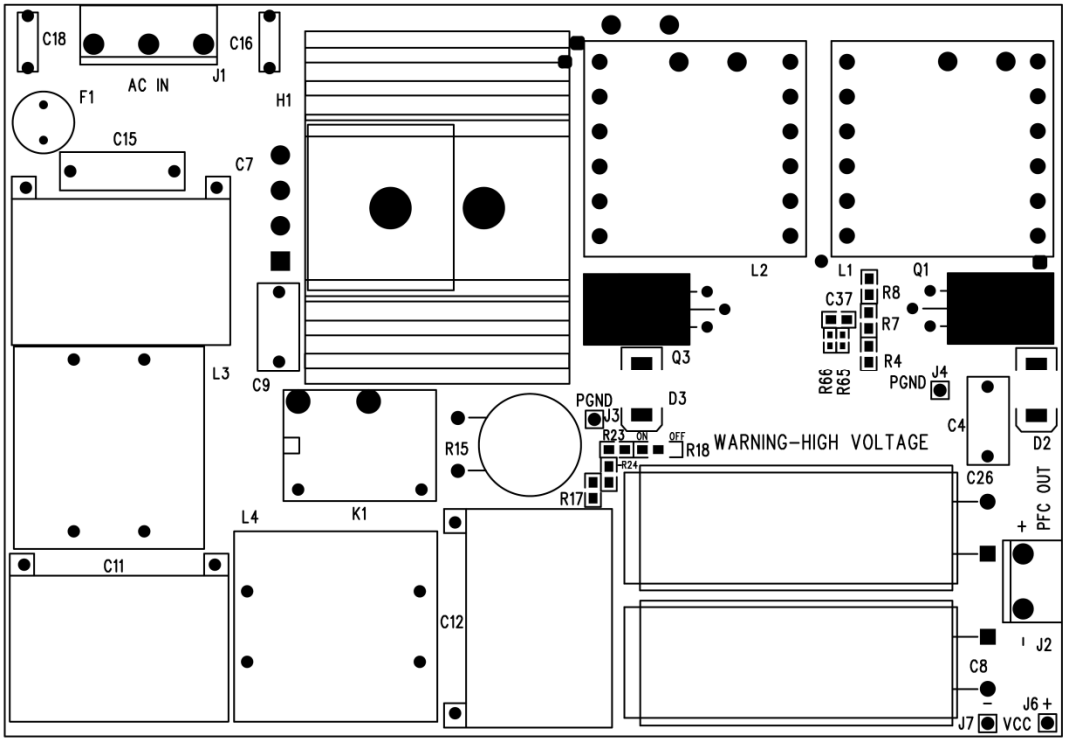


Figure 13. Top Assembly

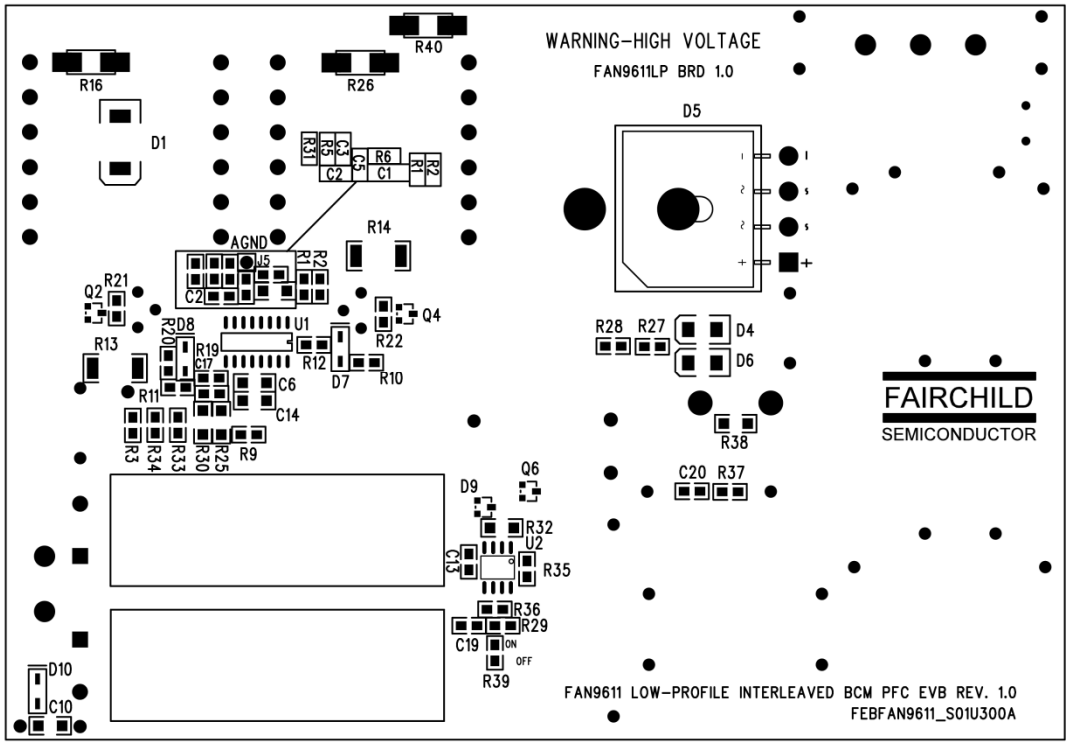


Figure 14. Bottom Assembly

8. Bill of Materials (BOM)

Item	Qty.	Reference	Part Number	Value	Description	Manufacturer	Package
1	2	C1, C6		0.22µF	CAP, SMD, Ceramic, 25V, X7R	STD	1206
2	1	C2		390nF	CAP, SMD, Ceramic, 25V, X7R	STD	805
3	2	C3, C13		15nF	CAP, SMD, Ceramic, 25V, X7R	STD	805
4	2	C4, C9	ECW-F2W154JAQ	150nF	Cap, 450V, 5%, Polypropylene	Panasonic	Thru-Hole
5	1	C5		470nF	CAP, SMD, Ceramic, 25V, X7R	STD	805
6	2	C7, C11	B32914A3474	470nF	Cap, 330VAC, 10%, Polypropylene	EPCOS	Thru-Hole
7	2	C8, C26	B43041A5157M	150µF	Cap, Alum, Elect.	EPCOS	Thru-Hole
8	2	C10, C14		2.2µF	CAP, SMD, Ceramic, 25V, X7R	STD	1206
9	1	C12	B32914A3105K	1µF	Cap, 330V_{AC}, 10%, Polypropylene	Epcos	Thru-Hole
10	1	C15	PHE840MB6100MB05R17	0.1µF	Cap, X Type, 10%, Polypropylene	KEMET	Thru-Hole
11	2	C16, C18	CS85-B2GA471KYNS	470pF	Cap, Ceramic, 250V_{AC}, 10%, Y5P,	TDK Corporation	Thru-Hole
12	1	C17		2.7nF	CAP, SMD, Ceramic, 25V, X7R	STD	805
13	1	C19		0.1µF	CAP, SMD, Ceramic, 25V, X7R	STD	805
14	1	C20		1µF	CAP, SMD, Ceramic,50V, X5R	STD	805
15	1	C37		1nF	CAP, SMD, Ceramic, 25V, X7R	STD	805
16	3	D1-3	ES3J		Diode, 600V, 3A, Ultra-Fast Recovery	Fairchild Semiconductor	SMC
17	2	D4, D6	S1J		Diode, General Purpose, 1A, 600V	Fairchild Semiconductor	SMA
18	1	D5	GBU6J		Diode, Bridge, 6A, 1000V	Fairchild Semiconductor	Thru-Hole
19	3	D7-8, D10	MBR0540		Diode, Schottky,40V, 500mA	Fairchild Semiconductor	SOD-123
20	1	D9	MMBZ5231B	5.1V	Diode, Zener, 5V, 350mW	Fairchild Semiconductor	SOT-23
21	1	F1	37421000410	10A	Fuse, 374 Series, 5.08mm Spacing	Littlefuse	Radial
22	1	H1	7-345-2PP-BA		Heatsink, Low Profile, T0-247	CTS	Thru-Hole
23	1	J1	1-1318301-3		Header, 3 Pin, 0.312 Spacing	TE Connectivity	Thru-Hole
24	1	J2	1-1123724-2		Header, 2 Pin, 0.312 Spacing	TYCO	Thru-Hole
25	5	J3-7	3103-2-00-21-00-00-08-0		Test pin, Gold, 40mil,	Mill-Max	Thru-Hole
26	1	K1	G5CA-1A DC12		RELAY PWR SPST-NO 10A 12VDC PCB	Omeron Electronics, Inc.	Thru-Hole
27	2	L1-2	750340834/NP1138-01	280µH	Inductor, Coupled	Wurth	Thru-Hole
28	2	L3-4	750311795	9mH	Common Mode Choke, 9mH	Wurth	Thru-Hole
29	2	Q1, Q3	FDP22N50N		MOSFET, NCH, UniFET, 500V, 11.5A, 0.18Ω	Fairchild Semiconductor	TO-220

Continued on the following page…

Item	Qty.	Reference	Part Number	Value	Description	Manufacturer	Package
30	2	Q2, Q4	ZXTP25020DFL		Transistor, PNP, 20V, 1.5A	Zetex	SOT-23
31	1	Q6	2N7002		MOSFET, NCH, 60V, 300mA	Philips	SOT-23
32	2	R1-2		46.4kΩ	RES, SMD, 1/8W	STD	805
33	6	R3, R18, R23-24 R33-34		665kΩ	RES, SMD, 1/8W	STD	805
34	3	R4, R7-8		340kΩ	RES, SMD, 1/8W	STD	805
35	1	R5		68.1kΩ	RES, SMD, 1/8W	STD	805
36	1	R6		60.4kΩ	RES, SMD, 1/8W	STD	805
37	1	R9		422kΩ	RES, SMD, 1/8W	STD	805
38	2	R10, R20		47.5Ω	RES, SMD, 1/8W	STD	805
39	2	R11-12		12Ω	RES, SMD, 1/8W	STD	805
40	2	R13-14		0.033Ω	RES, SMD, 1W	STD	2512
41	1	R15	B57237S0330M000	33Ω	Thermistor	Epcos Inc.	Thru-Hole
42	3	R16, R26, R40		0Ω	RES, SMD, 1/2W	STD	2010
43	1	R17		45.3kΩ	RES, SMD, 1/8W	STD	805
44	1	R19		15.4kΩ	RES, SMD, 1/8W	STD	805
45	2	R21-22		10kΩ	RES, SMD, 1/8W	STD	805
46	1	R25		24.9kΩ	RES, SMD, 1/4W	STD	1206
47	2	R27-28		1.24MΩ	RES, SMD, 1/8W	STD	805
48	3	R29, R35-36		1.2kΩ	RES, SMD, 1/8W	STD	805
49	1	R30		23.7kΩ	RES, SMD, 1/4W	STD	1206
50	1	R31		7.68kΩ	RES, SMD, 1/8W	STD	805
51	1	R32		150kΩ	RES, SMD, 1/4W	STD	1206
52	1	R37		1kΩ	RES, SMD, 1/8W	STD	805
53	1	R38		0Ω	RES, SMD, 1/4W	STD	1206
54	1	R39		0Ω	RES, SMD, 1/8W	STD	805
55	2	R65-66		DNP	RES, SMD, 1/10W	STD	603
56	1	U1	FAN9611		Interleaved, Dual, BMC, PFC Controller	Fairchild Semiconductor	SOIC-16
57	1	U2	LM393M		Dual, Differential Comparator	Fairchild Semiconductor	SOIC-8
58	2	SC1, SC2	PMSSS 440 0050 PH		SCREW MACHINE PHIL 4-40X1/2 SS	STD	Hardware
59	2	W1, W2	INT LWZ 004		WASHER LOCK INT TOOTH #4 ZINC	STD	Hardware
60	2	N1, N2	HNZ440		NUT HEX 4-40 ZINC PLATED	STD	Hardware
61	1	PWB			4 Layer, FR4, FAN9611 LOW-PROFILE PWB - REV. 1.0	Fairchild Semiconductor	PCB

Notes:
1. DNP = Do Not Populate
2. STD = Standard Components

9. Inrush Current Limiting

The evaluation board includes an inrush current limiting circuit comprised of the highlighted components shown in Figure 15.

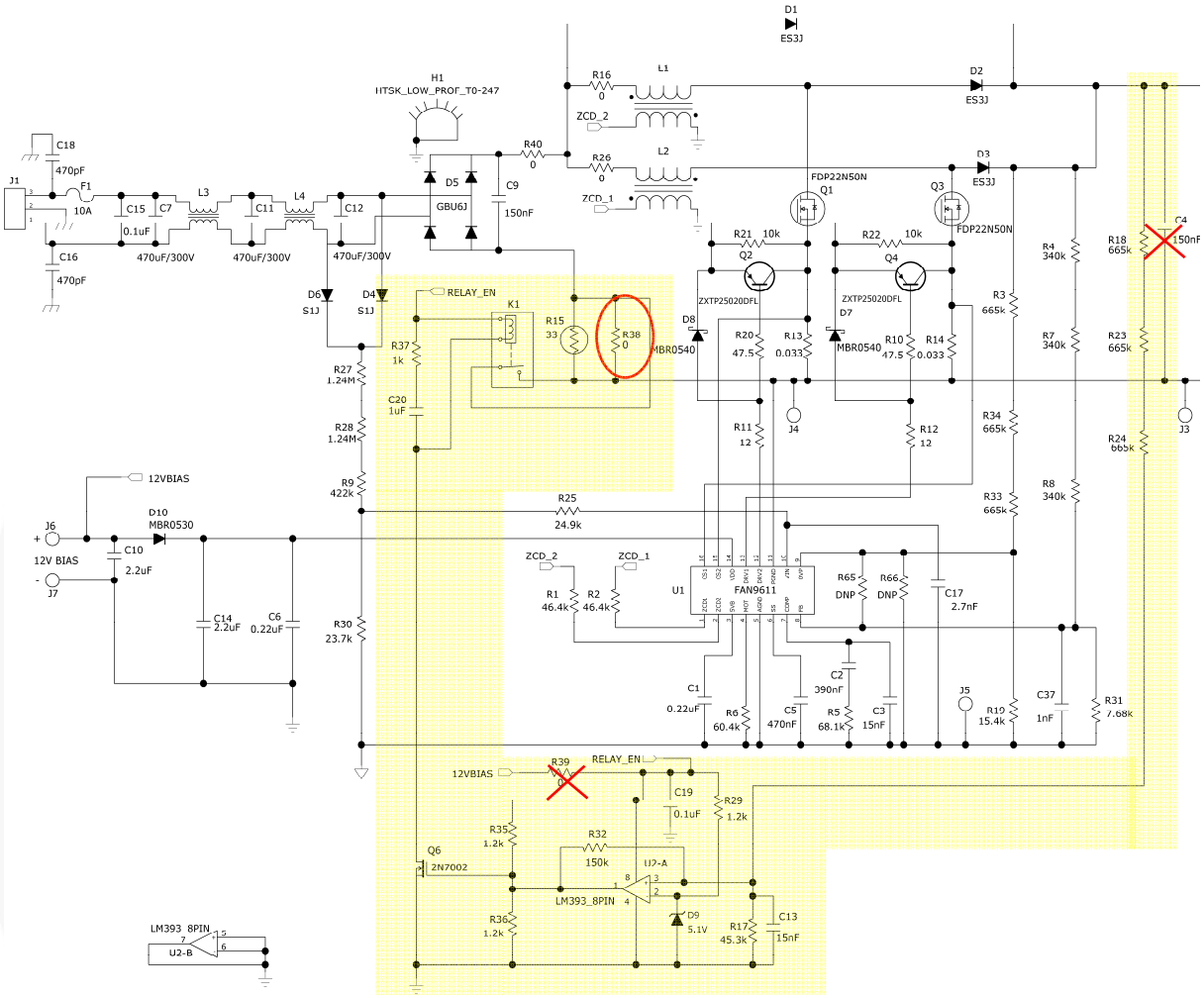
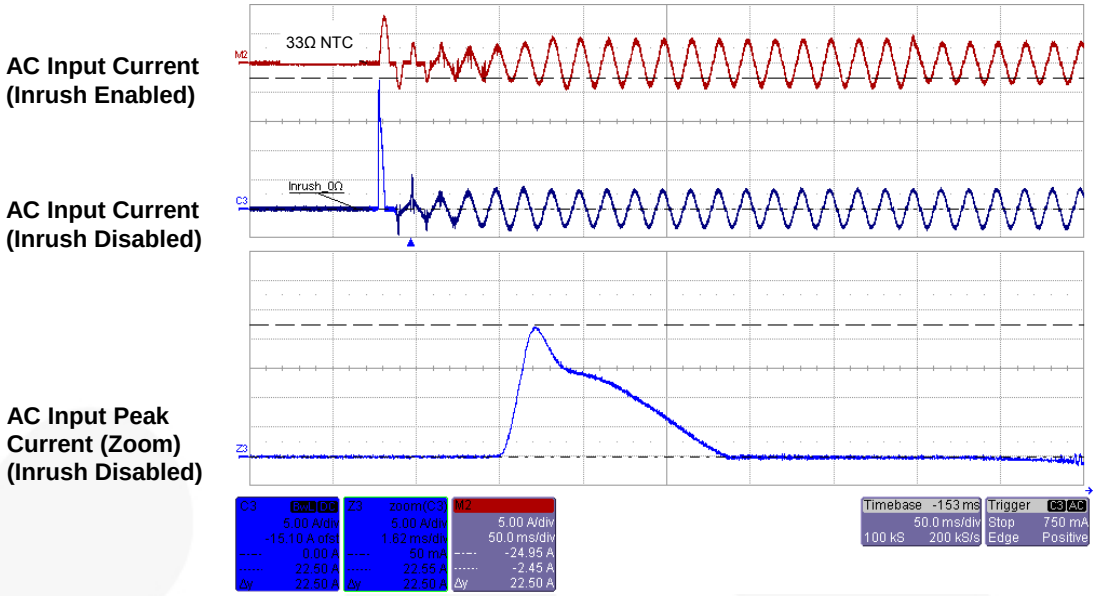


Figure 15. Inrush Current Limiting Circuit

Since the inrush current limiting circuit has a negative impact on light-load efficiency and may not be required by all offline applications, the evaluation board is configured with the inrush circuit fully populated, but disabled, as shown in Figure 15. R18 and R39 are installed on the PCB; purposely electrically open. To enable and test the inrush current limiting circuit, rotate R18 and R39 to complete the proper series connection shown in the schematic. Remove R38 to allow the 33Ω NTC thermistor (R15) to limit the inrush current during startup. Input current measurements can be made by removing the R16, 0Ω jumper and installing a loop of wire connected to the holes provided within the R16 PCB pad locations. A current probe can then be connected to the wire loop. The effectiveness of the inrush current limiting function is shown below in Figure 16.



M2: AC Line Current (5A/div), CH3: AC Line Current (5A/div), Time (50ms/div)

Figure 16. Full-Load Startup at 115V_{AC}

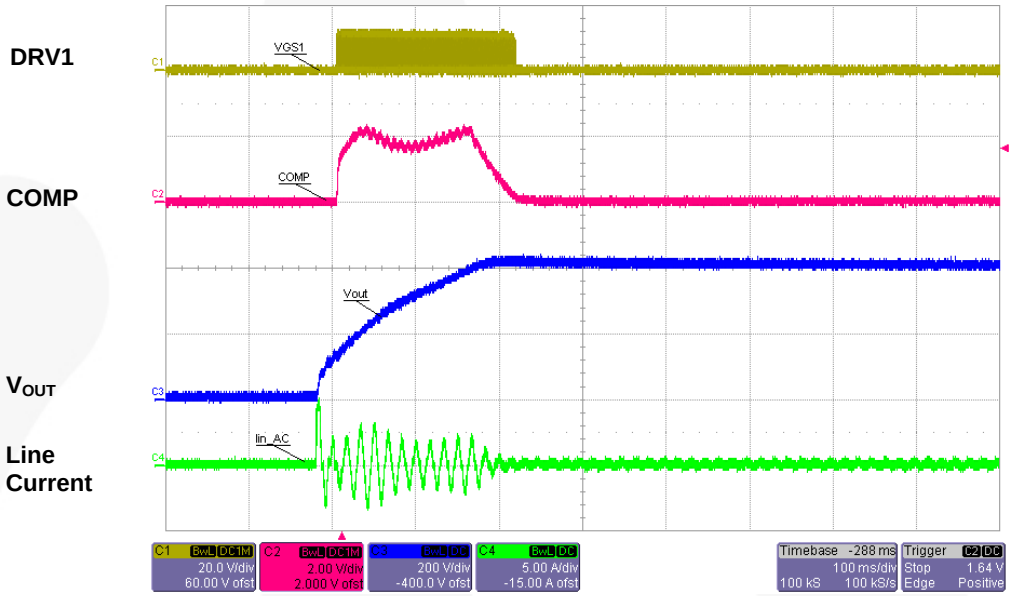
Table 4. Inrush Current Limiting Circuit Effectiveness Comparison

Input Line Voltage	Output Power	Peak Line Current (Inrush Circuit Disabled)	Peak Line Current (Inrush Circuit Enabled)	% Inrush Current Reduction
V_{IN}=115V_{AC}	300W	22.50A_{PK}	8.45A_{PK}	62.40%
V_{IN}=230V_{AC}	300W	26.9A_{PK}	11.5A_{PK}	57.3%

10. Test Results

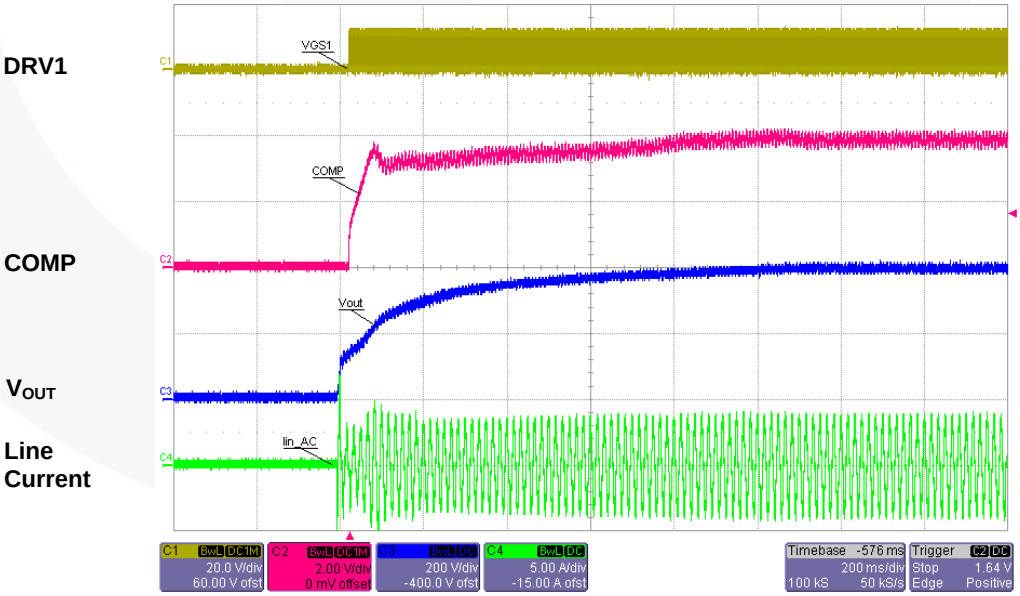
10.1. Startup

Figure 17 and Figure 18 show the startup operation at $115V_{AC}$ line voltage for no-load and full-load condition, respectively. Due to the closed-loop soft-start, almost no overshoot is observed for no-load startup and full-load startup.



CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (5A/div), Time (100ms/div)

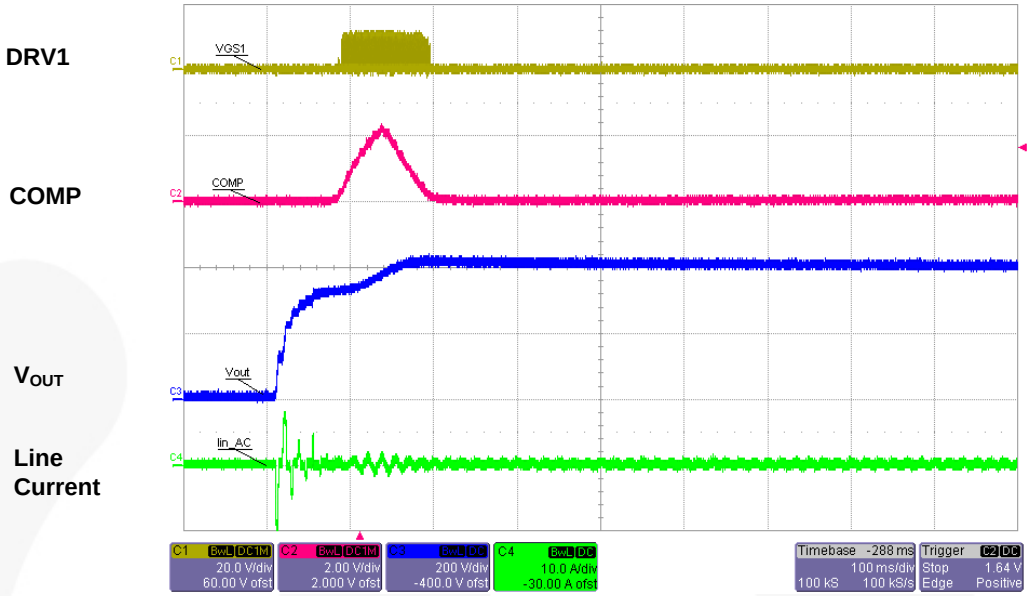
Figure 17. No-Load Startup at $115V_{AC}$



CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (5A/div), Time (200ms/div)

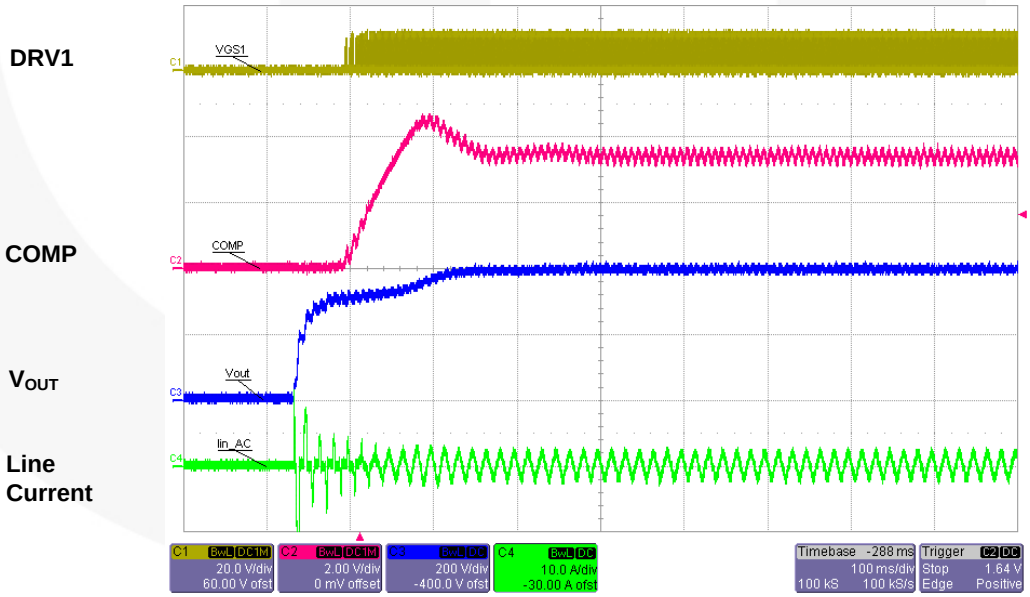
Figure 18. Full-Load Startup at $115V_{AC}$

Figure 19 and Figure 20 show the startup operation at $230V_{AC}$ line voltage for no-load and full-load conditions, respectively. Due to the closed-loop soft-start, almost no overshoot is observed for no-load startup and full-load startup.



CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (10A/div), Time (100ms/div)

Figure 19. No-Load Startup at $230V_{AC}$

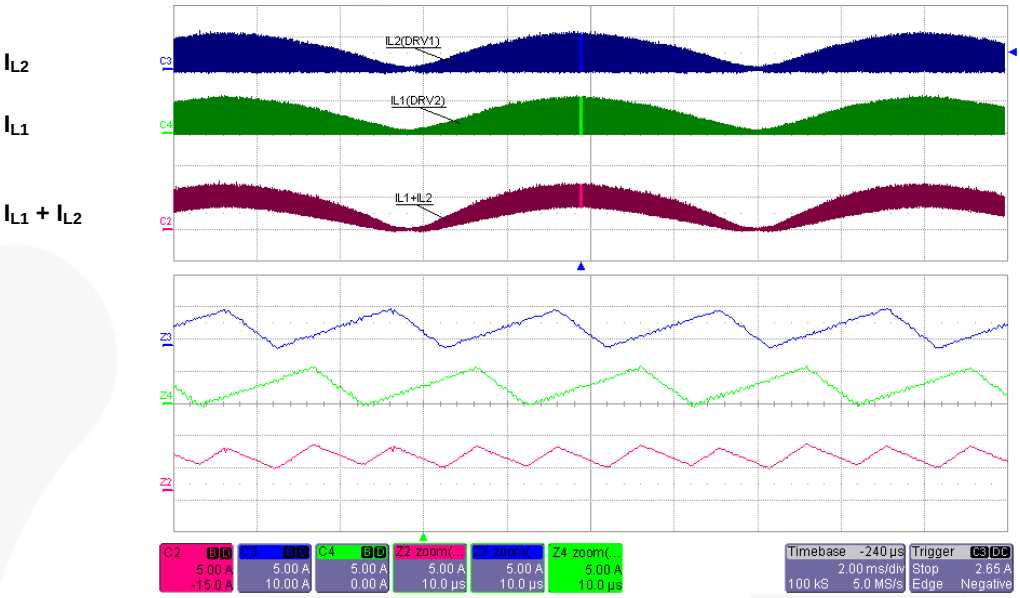


CH1: Gate Drive 1 Voltage (20V/div), CH2: COMP Voltage (2V/div),
CH3: Output Voltage (200V/div), CH4: Line Current (10A/div), Time (100ms/div)

Figure 20. Full-Load Startup at $230V_{AC}$

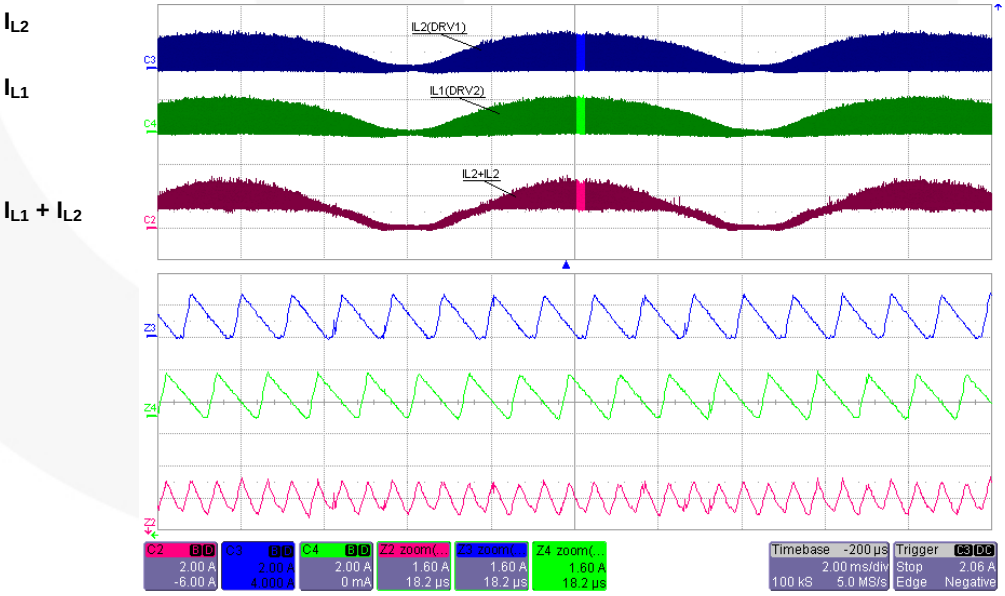
10.2. Steady-State Operation

Figure 21 and Figure 22 show the two inductor currents and the sum of the two inductor currents operating at full load for $90V_{AC}$ and $230V_{AC}$ line voltage. The sum of the inductor currents has relatively small ripple due to the ripple cancellation of interleaving.



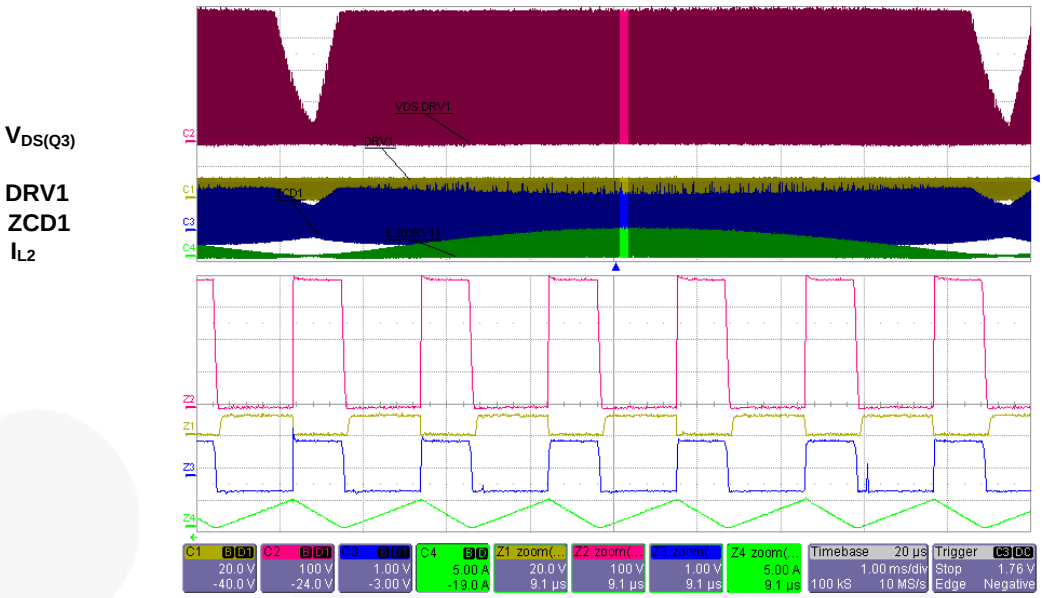
CH3: Inductor L2 Current (5A/div), CH4: Inductor L1 Current (5A/div),
CH2: Sum of Two Inductor Currents (5A/div), Time (2ms/div, zoom to 10µs/div)

Figure 21. Zoom of Inductor Current Waveforms at Full-Load and $90V_{AC}$



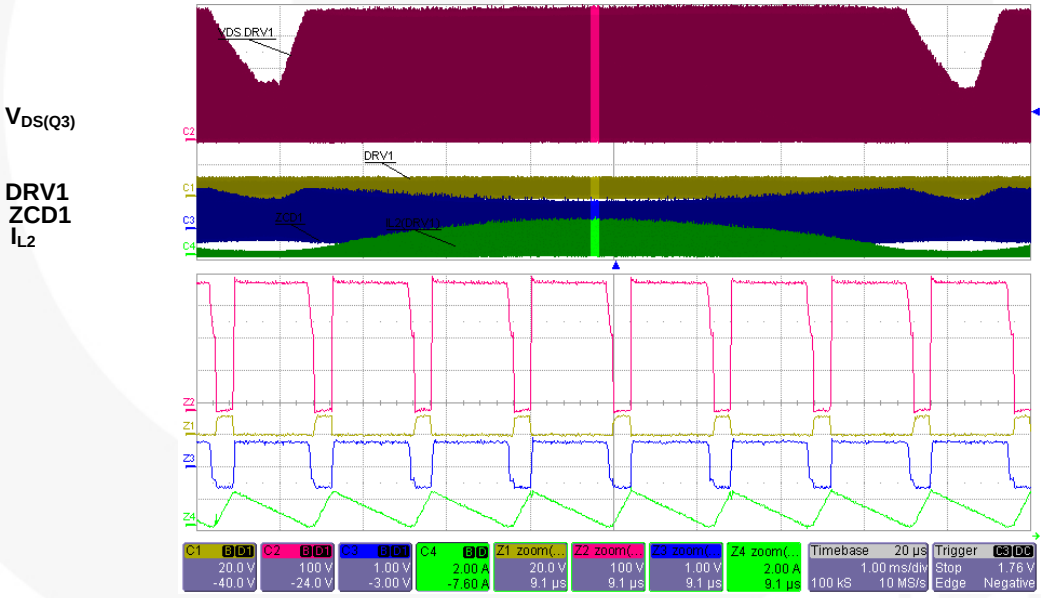
CH3: Inductor L1 Current (2A/div), CH4: Inductor L2 Current (2A/div),
CH2: Sum of Two Inductor Current (2A/div), Time (2ms/div)

Figure 22. Zoom of Inductor Current Waveforms at Full-Load and $230V_{AC}$



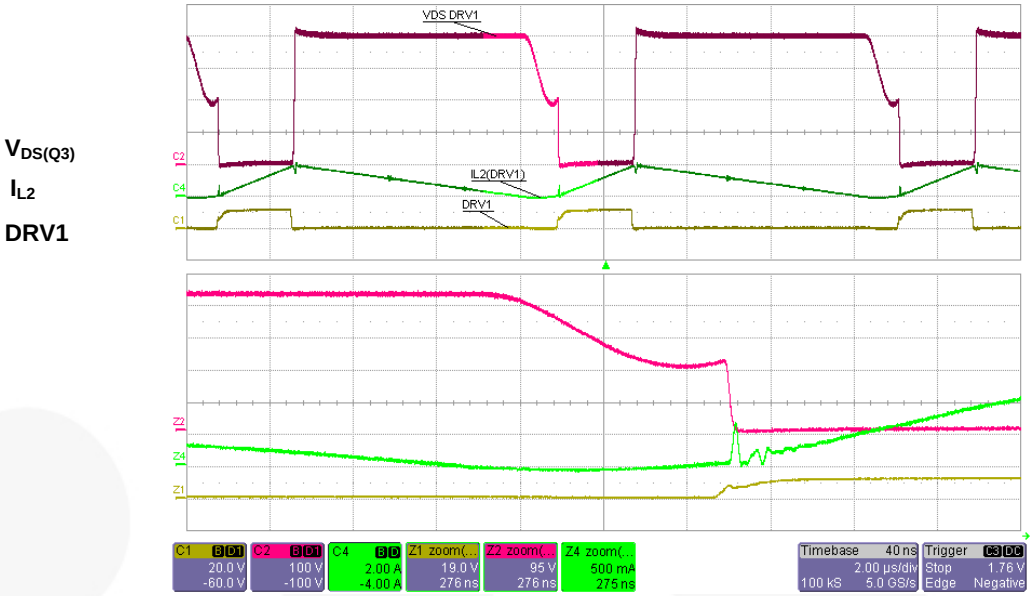
CH1: DRV1 (20V/div), CH2: VDS(Q3) (100V/div)
CH3: ZCD1 (1V/div), CH4: Inductor L2 Current (5A/div)

Figure 23. Zero Valley Switching at Full Load, 115V_{AC}



CH1: DRV1 (20V/div), CH2: VDS(Q3) (100V/div)
CH3: ZCD1 (1V/div), CH4: Inductor L2 Current (5A/div)

Figure 24. Zero Valley Switching at Full Load, 230V_{AC}



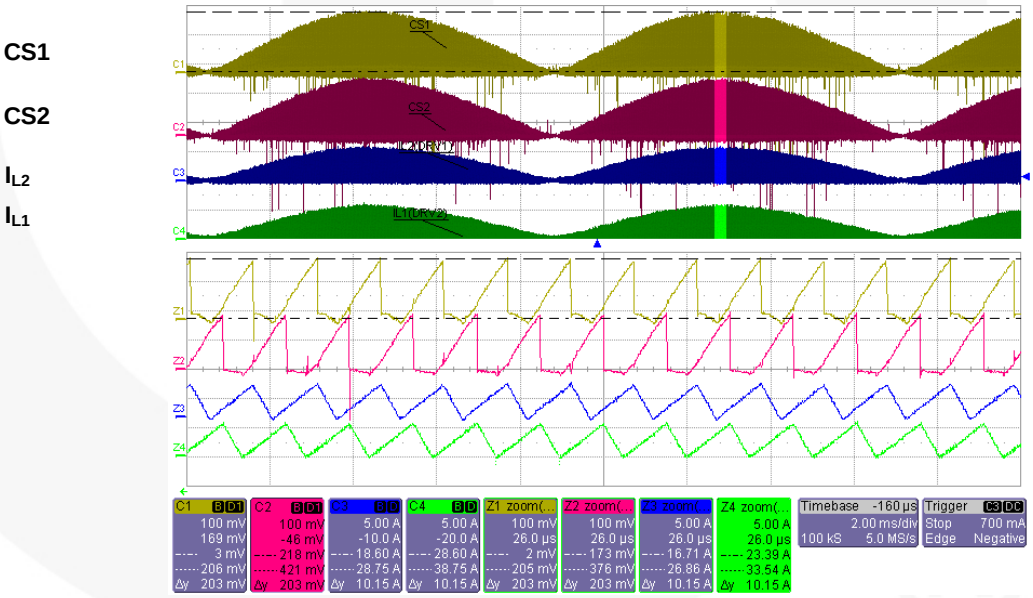
$V_{DS(Q3)}$

I_{L2}

DRV1

CH1: DRV1 (20V/div), CH2: VDS(Q3) (100V/div)
CH4: Inductor L2 Current (5A/div)

Figure 25. Zoom of Valley Switching at Full Load, 230V_{AC}



$CS1$

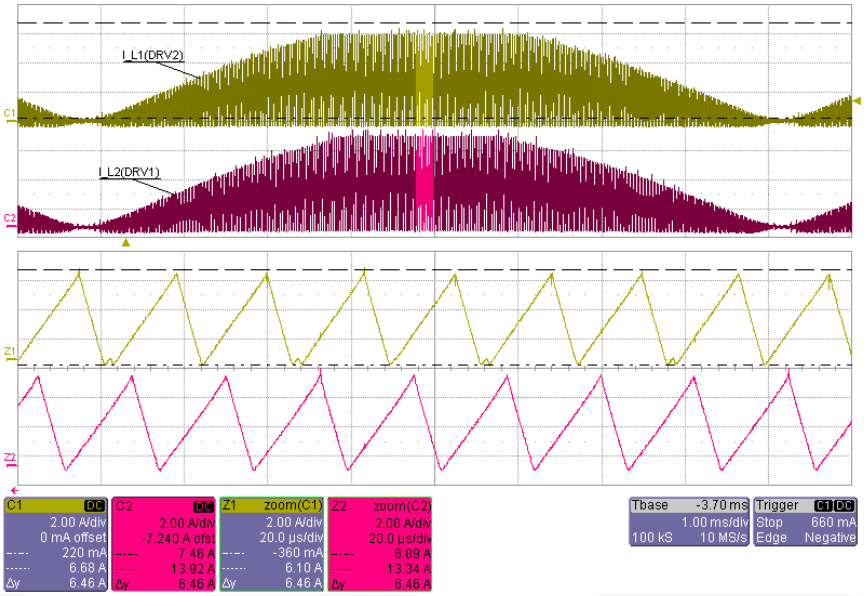
$CS2$

I_{L2}

I_{L1}

CH1: FAN9611, Pin 16 (100mV/div), CH2: FAN9611, Pin 15 (100mV/div)
CH3: Inductor L2 Current (5A/div), CH4: Inductor L1 Current (5A/div)

Figure 26. Current-Sense Waveforms at Full Load, 90V_{AC}

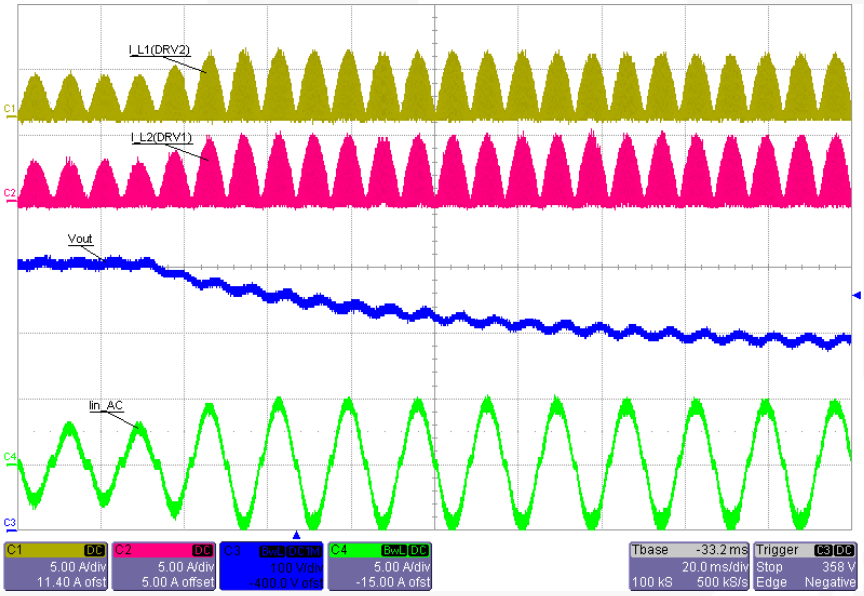


I_{L1}

I_{L2}

CH1: Inductor L1 Current (2A/div), CH2: Inductor L2 Current (2A/div)

Figure 27. Inductor Current Waveforms at 360W, 85V_{AC}, Over-Current Operation



I_{L1}

I_{L2}

Line Current

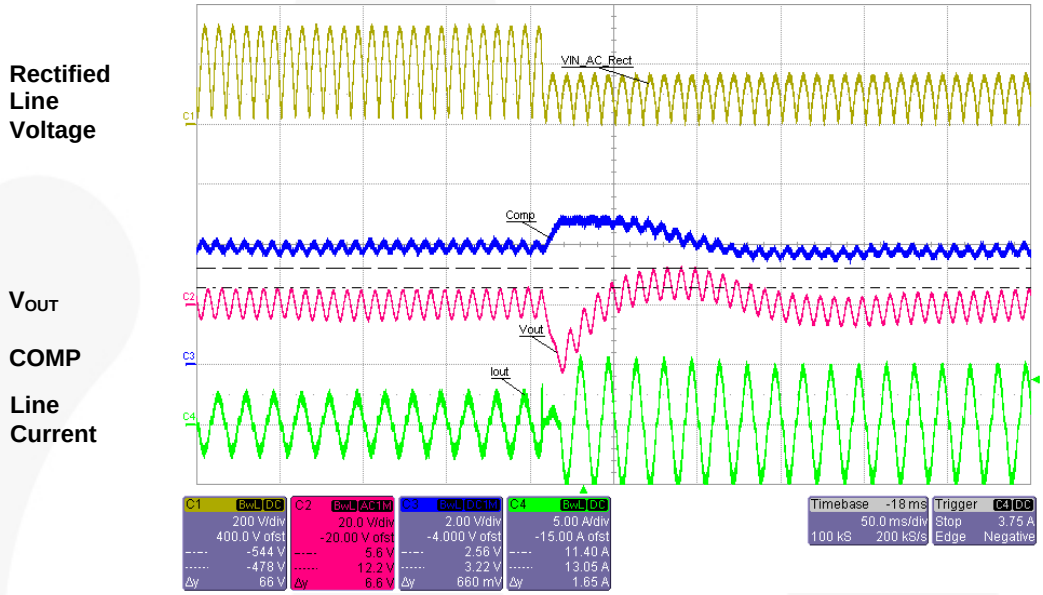
V_{OUT}

CH1: Inductor L1 Current (5A/div), CH2: Inductor L2 Current (5A/div)
CH3: Output Voltage (100V/div), CH4: Line Current (5A/div), Time (20ms/div)

Figure 28. MOT Power Limit, 0.5A to 1.3A Load Transient, 115V_{AC}

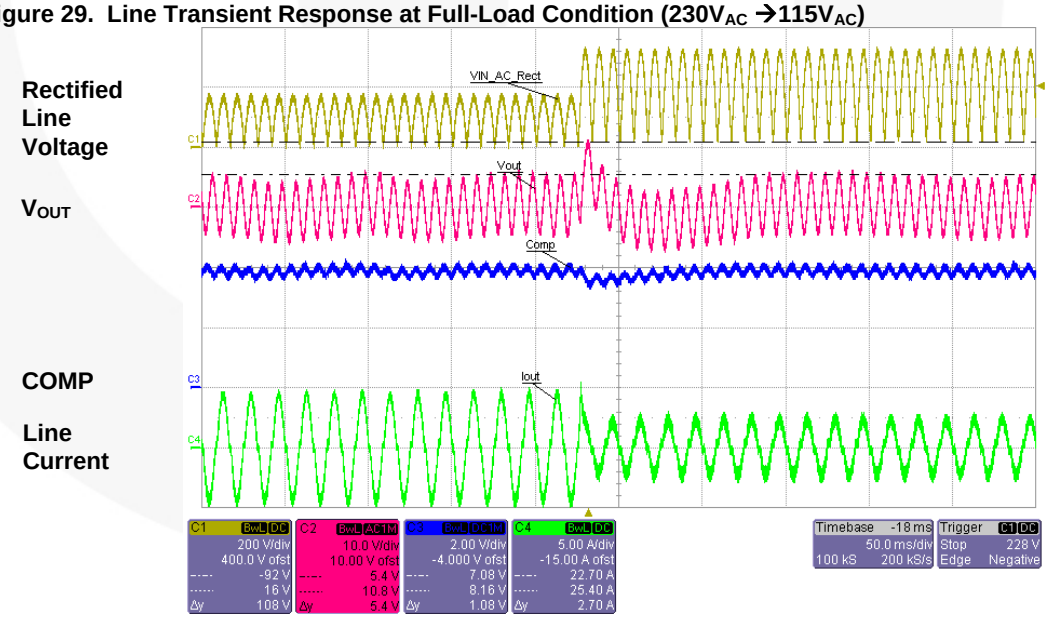
10.3. Line Transient

Figure 29 and Figure 30 show the line transient operation and minimal effect on output voltage due to the line feed-forward function. When the line voltage changes from $230V_{AC}$ to $115V_{AC}$, about 20V (5% of nominal output voltage) voltage undershoot is observed. When the line voltage changes from $115V_{AC}$ to $230V_{AC}$, about 6V (1.5% of nominal output voltage) voltage overshoot is observed.



CH1: Rectified Line Voltage (200V/div), CH2: Output Voltage (20V/div, AC),
CH3: COMP Voltage (2V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 29. Line Transient Response at Full-Load Condition ($230V_{AC}$ →$115V_{AC}$)

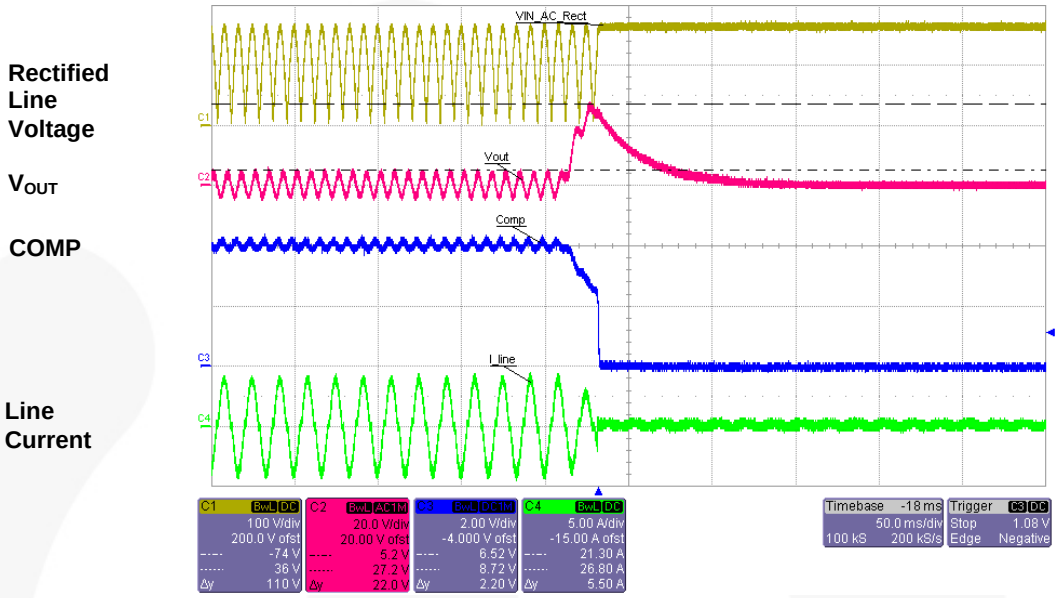


CH1: Rectified Line Voltage (200V/div), CH2: Output Voltage (10V/div, AC),
CH3: COMP Voltage (2V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 30. Line Transient Response at Full-Load Condition ($115V_{AC}$ →$230V_{AC}$)

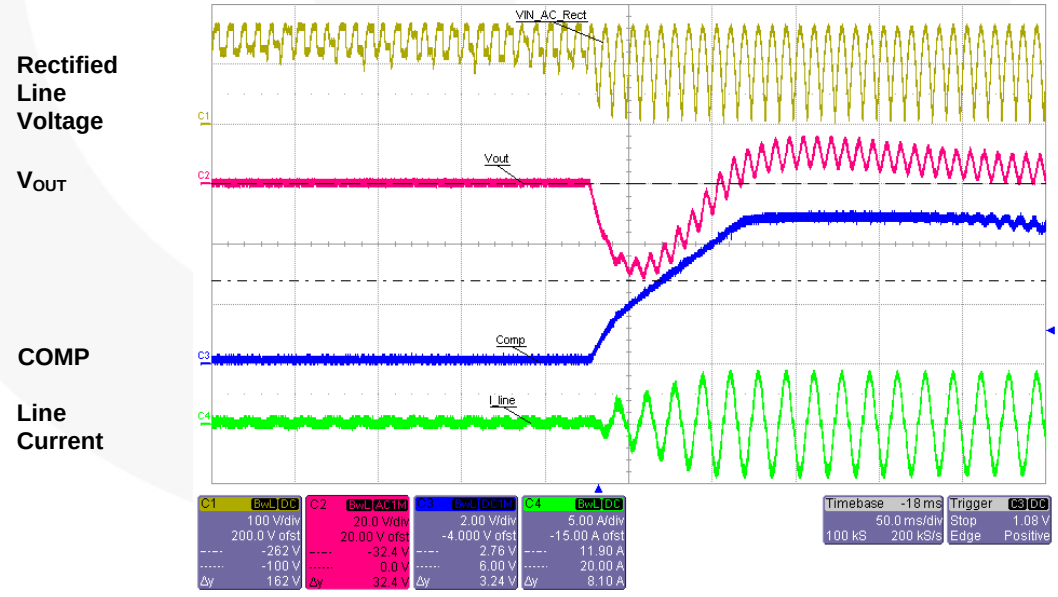
10.4. Load Transient

Figure 31 and Figure 32 show the load-transient operation. When the output load changes from 100% to 0%, 20V (5% of nominal output voltage) voltage overshoot is observed. When the output load changes from 0% to 100%, 34V (8.5% of nominal output voltage) voltage undershoot is observed.



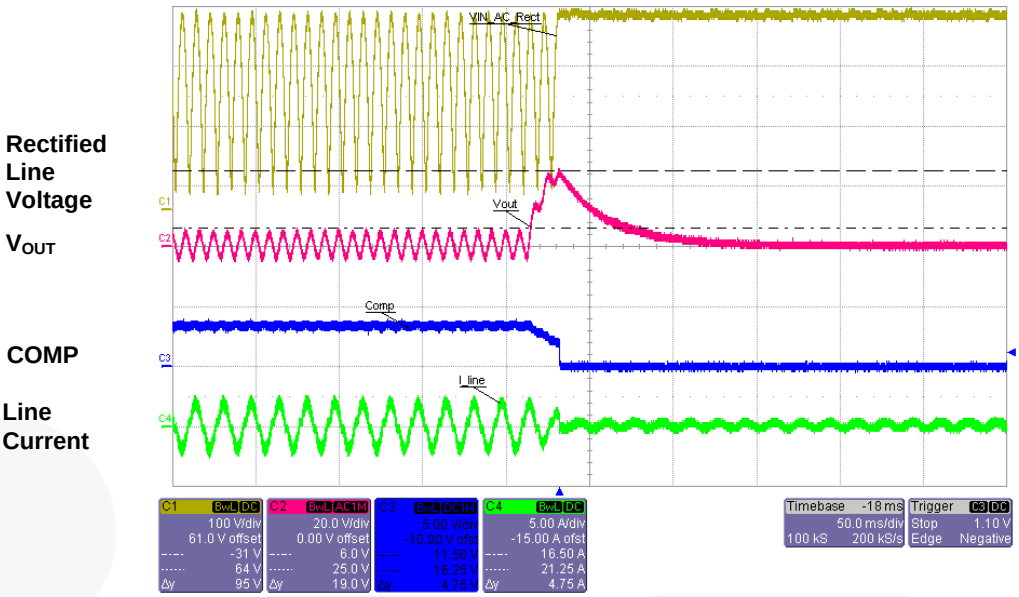
CH1: Rectified Line Voltage (100V/div), CH2: Output Voltage (20V/div, AC), CH3: COMP Voltage (2V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 31. Load Transient Response at 115V_{AC} (Full Load → No Load)



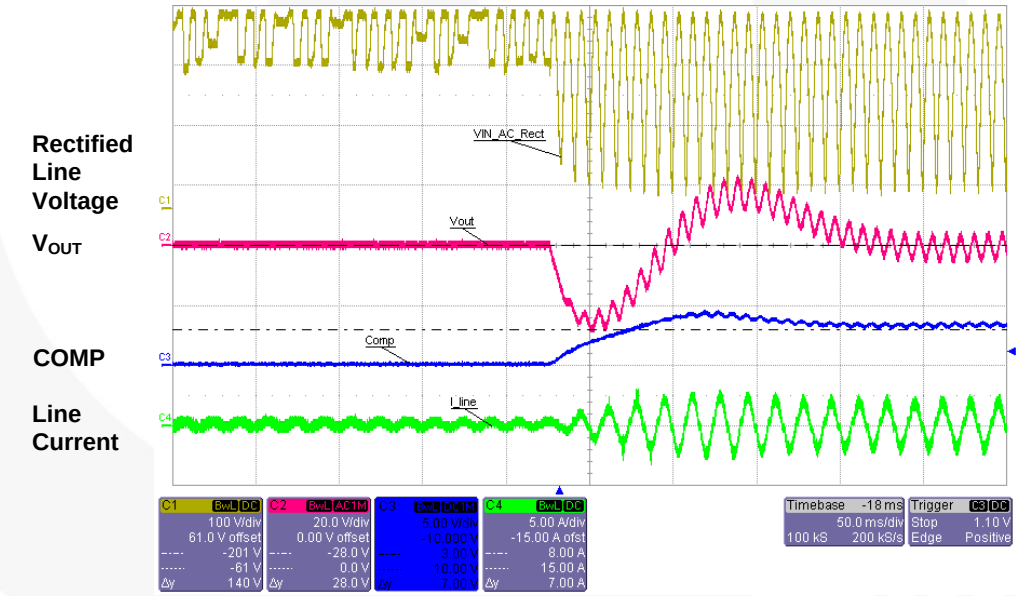
CH1: Rectified Line Voltage (100V/div), CH2: Output Voltage (20V/div, AC), CH3: COMP Voltage (2V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 32. Load Transient Response at 115V_{AC} (No Load → Full Load)



CH1: Rectified Line Voltage (100V/div), CH2: Output Voltage (20V/div, AC),
CH3: COMP Voltage (5V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 33. Load Transient Response at 230V_{AC} (Full Load → No Load)

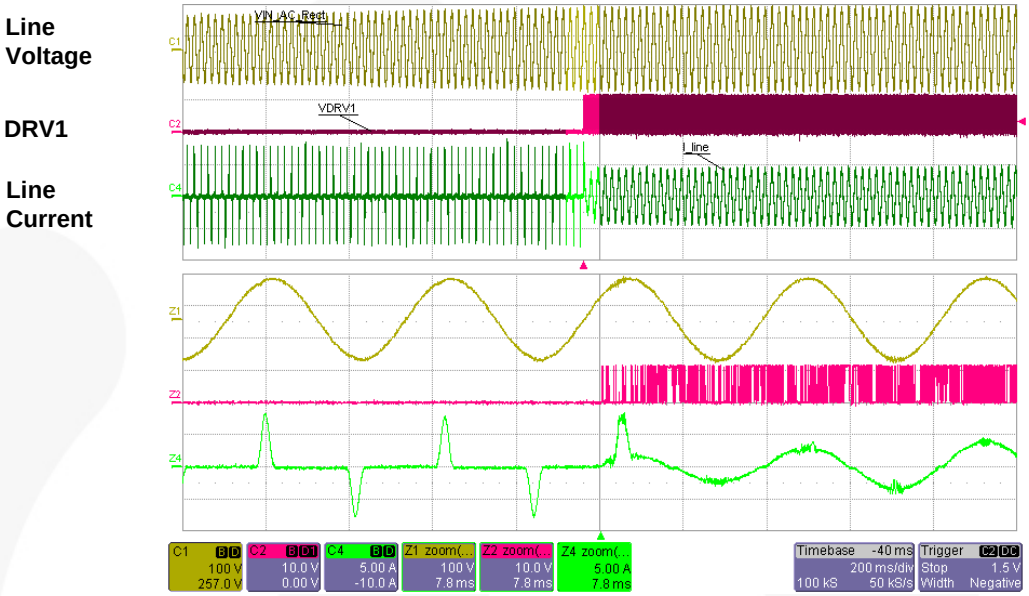


CH1: Rectified Line Voltage (100V/div), CH2: Output Voltage (20V/div, AC),
CH3: COMP Voltage (5V/div), CH4: Line Current (5A/div), Time (50ms/div)

Figure 34. Load Transient Response at 230V_{AC} (No Load → Full Load)

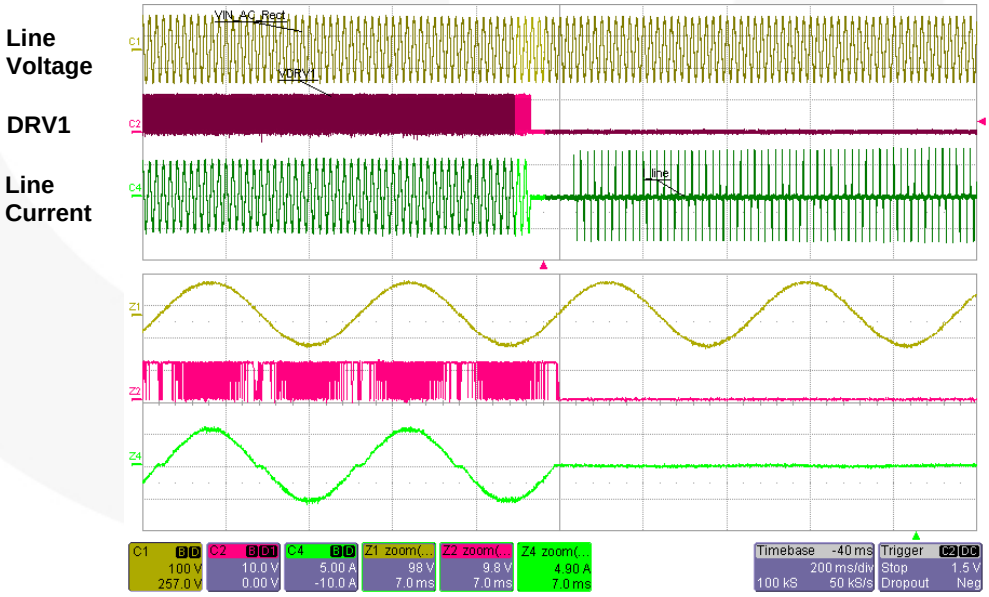
10.5. Brownout Protection

Figure 35 shows the startup operation while slowly increasing the line voltage. The power supply starts up when the line voltage reaches around $90V_{AC}$. Figure 36 shows the shutdown operation while slowly decreasing the line voltage. The power supply shuts down when the line voltage reaches around $80V_{AC}$.



CH1: Line Voltage (100V/div), CH2: Gate Drive 1 Voltage (10V/div),
CH4: Line Current (5A/div), Time (200ms/div)

Figure 35. Startup Slowly Increasing the Line Voltage

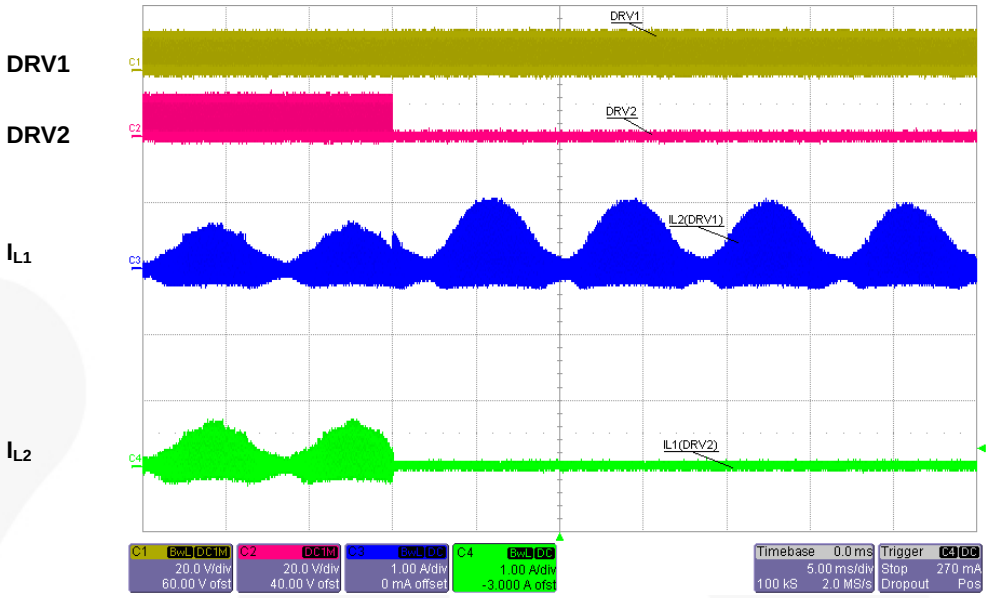


CH1: Line Voltage (100V/div), CH2: Gate Drive 1 Voltage (10V/div),
CH4: Line Current (5A/div), Time (20ms/div)

Figure 36. Shutdown Slowly Decreasing the Line Voltage

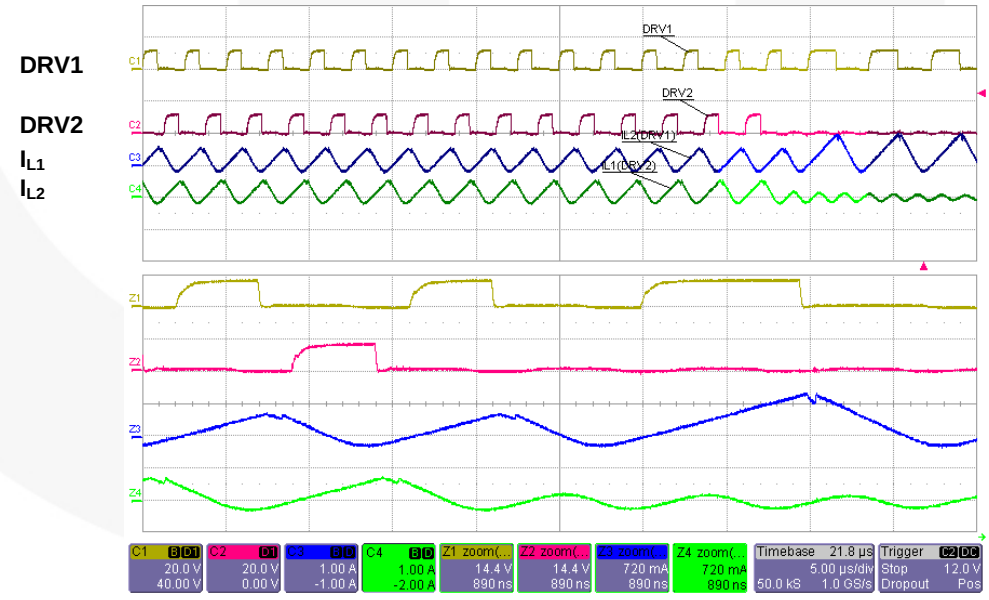
10.6. Phase Management

Figure 37 and Figure 38 show the phase-shedding waveforms. As observed, when the gate drive signal of Channel 2 is disabled, the duty cycle of Channel 1 gate drive signal is doubled to minimize the line current glitch and guarantee smooth transient.



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5ms/div)

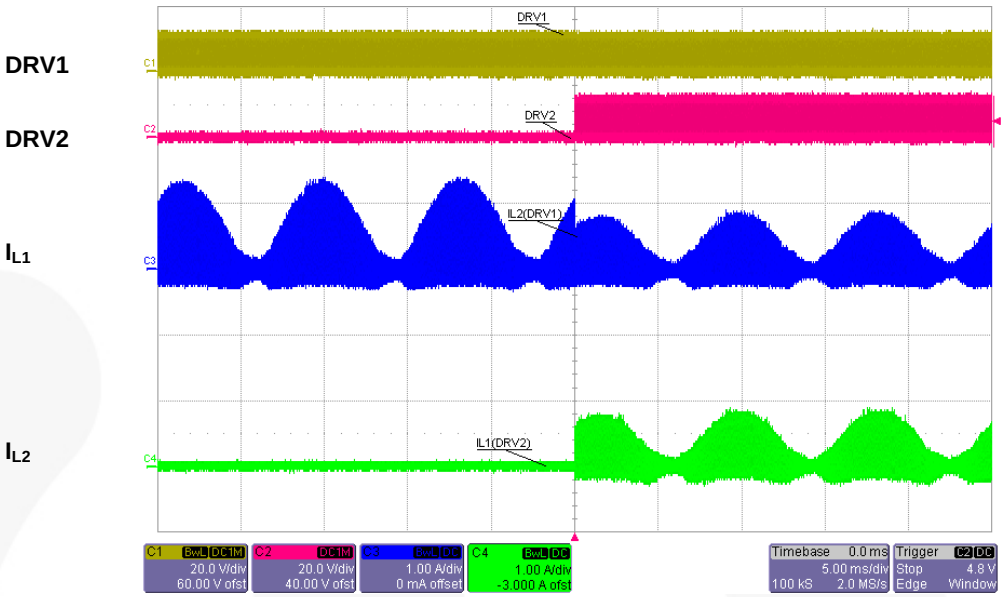
Figure 37. Phase-Shedding Operation



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5µs/div)

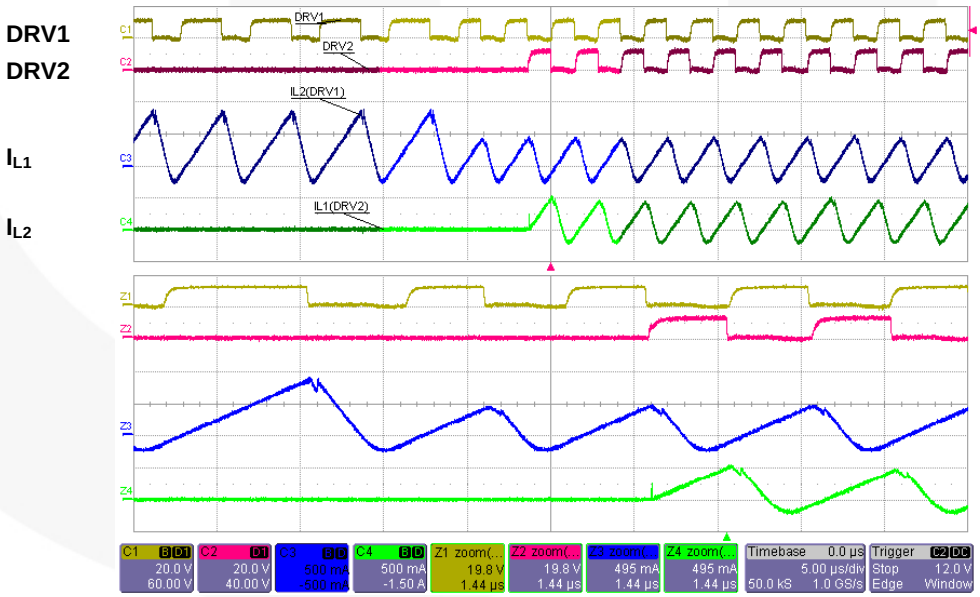
Figure 38. Phase-Shedding Operation (Zoomed-in Timescale)

Figure 39 and Figure 40 show the phase-adding waveforms. As observed, just before the Channel 2 gate drive signal is enabled, the duty cycle of Channel 1 gate drive signal is reduced by 50% to minimize the line current glitch and guarantee smooth transient. In Figure 40, the first pulse of gate drive 2 during the phase-adding operation is skipped to ensure 180° out-of-phase interleaving operation during transient.



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5ms/div)

Figure 39. Phase-Adding Operation



CH1: Gate Drive 1 Voltage (20V/div), CH2: Gate Drive 2 Voltage (20V/div),
CH3: Inductor L1 Current (1A/div), CH4: Inductor L2 Current (1A/div), Time (5µs/div)

Figure 40. Phase-Adding Operation (Zoomed-in Timescale)

10.7. Efficiency

Figure 41 and Figure 42 show the measured efficiency of the 300W evaluation board with R_{MOT}=60.4kΩ at input voltages of $115V_{AC}$ and $230V_{AC}$. The phase management threshold on the test evaluation board is approximately 15% of the nominal output power. The threshold can be adjusted upwards to achieve a more desirable efficiency profile by increasing the MOT resistor. Figure 43 and Figure 44 show the light-load efficiency improvement that can be achieved when the threshold is adjusted to 30% by increasing the MOT resistor to 120kΩ.

Since phase shedding reduces the switching loss by effectively decreasing the switching frequency at light load, greater efficiency improvement is achieved at $230V_{AC}$, where switching losses dominate. Relatively less improvement is obtained at $115V_{AC}$, since the MOSFET is turned on with zero voltage and switching losses are negligible. The efficiency measurements include the losses in the EMI filter, cable loss and power consumption of the control IC.

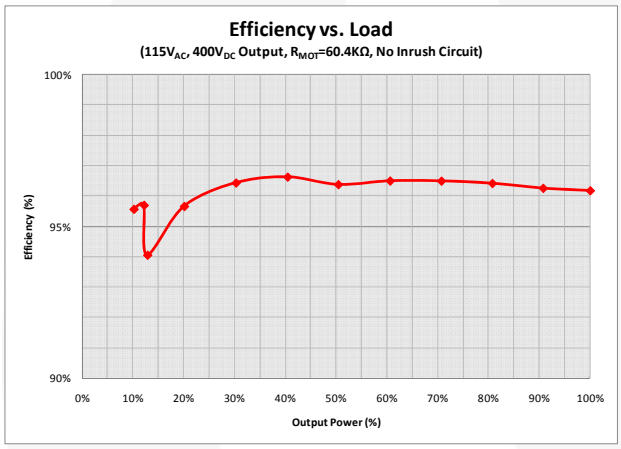


Figure 41. Efficiency vs. Load ($115V_{AC}$)

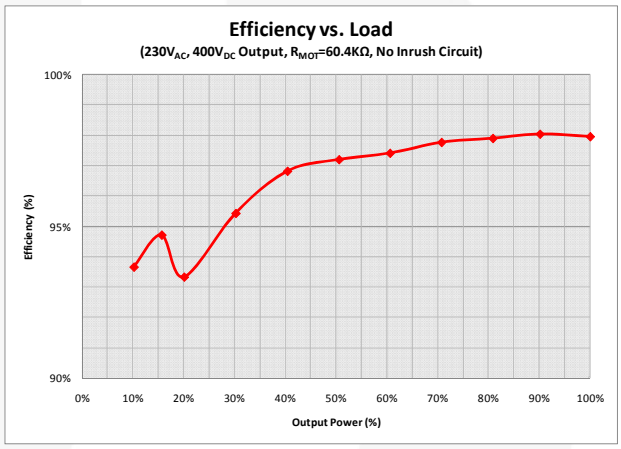


Figure 42. Efficiency vs. Load ($230V_{AC}$)

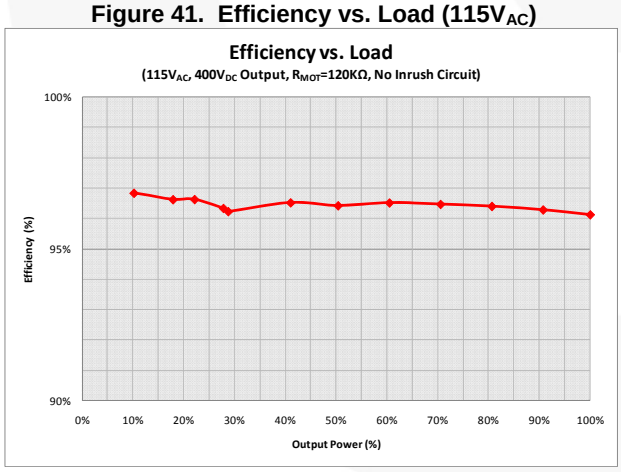


Figure 43. Efficiency vs. Load ($115V_{AC}$)

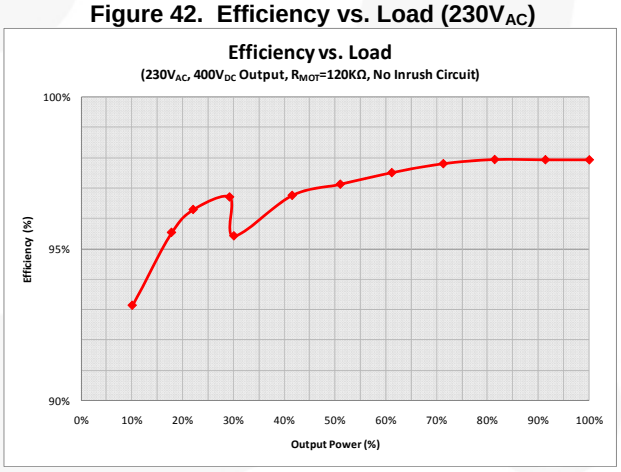


Figure 44. Efficiency vs. Load ($230V_{AC}$)

Figure 45 and Figure 46 show a direct comparison of light-load efficiency benefit gained when increasing the MOT resistor. For R_{MOT}=120kΩ, the phase threshold is adjusted upward from 18% to approximately 30% of nominal maximum output power. It is not recommended to adjust the phase threshold near the 50% nominal maximum output power, since each individual BCM PFC channel is optimally designed to process 50% (plus 20% margin) of the total output power required by the load.

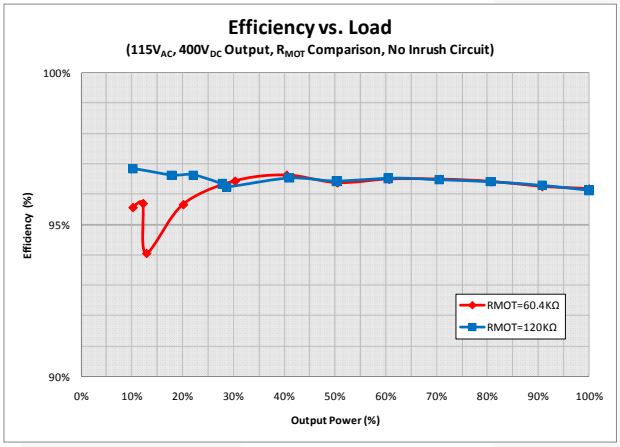


Figure 45. Efficiency vs. Load ($115V_{AC}$)

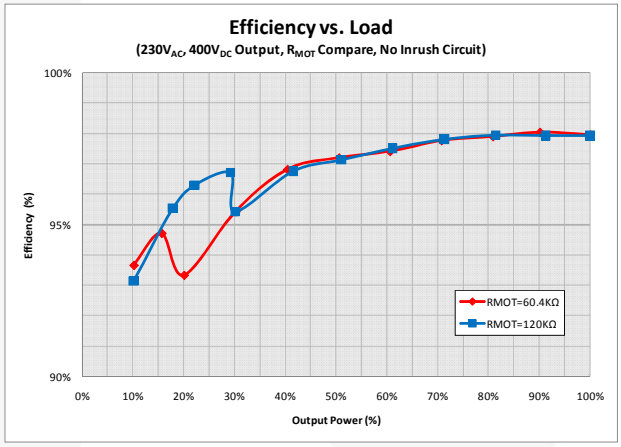


Figure 46. Efficiency vs. Load ($230V_{AC}$)

The FEBFAN9611_S01U300A evaluation board is configured with R_{MOT}=60.4kΩ, which sets the maximum output power limit to about 360W. Because of the highly optimized, low-profile cross-section of this design; the EFD30 inductors are not rated to process more than 200W each (400W total output power). When the MOT resistor is increased to 120kΩ, the maximum allowable output power is also increased to greater than 400W. To fully protect the power stage, a simple voltage divider and PNP clamp should be applied to the FAN9611 COMP voltage (pin 7) as detailed in AN-6086, Figure 15.

10.8. Harmonic Distortion and Power Factor

Figure 47 and Figure 48 compare the measured harmonic current with EN61000 Class D and Class C, respectively, at input voltages of $115V_{AC}$ and $230V_{AC}$. Class D is applied to TV and PC power, while Class C is applied to lighting applications. As can be observed, both regulations are met with sufficient margin.

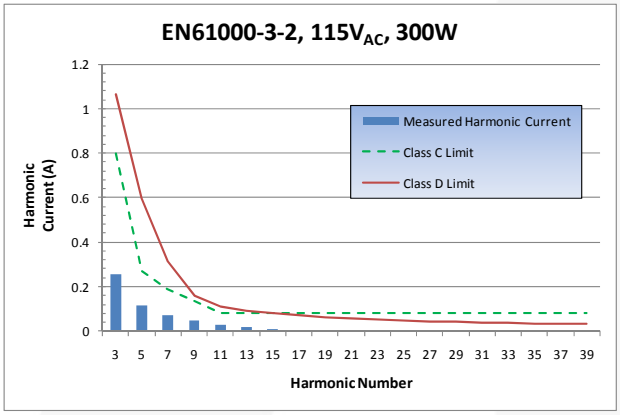


Figure 47. Harmonic Current, $115V_{AC}$

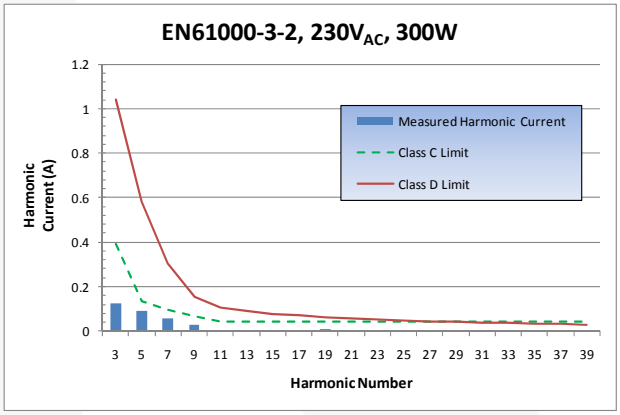


Figure 48. Harmonic Current, $230V_{AC}$

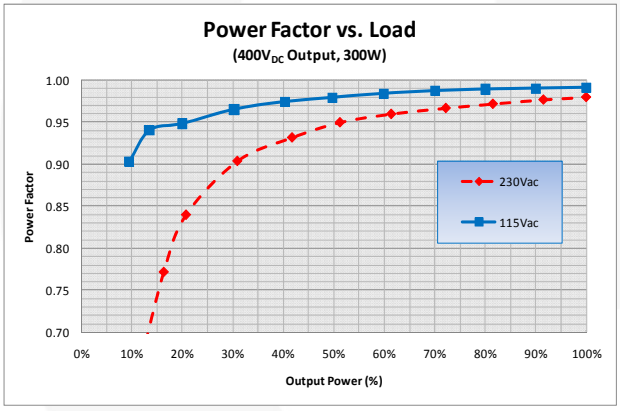


Figure 49. Measured Power Factor

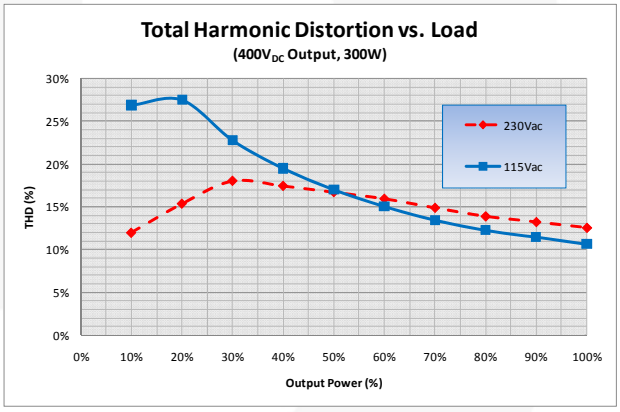


Figure 50. Measured Total Harmonic Distortion

Figure 49 shows the measured power factor at input voltage of $115V_{AC}$ and $230V_{AC}$. As observed, high power factor above 0.95 is obtained from 100% to 50% load. Figure 50 shows the total harmonic distortion at input voltages of $115V_{AC}$ and $230V_{AC}$.

10.9. EMI

EN55022 CISPR, Class B

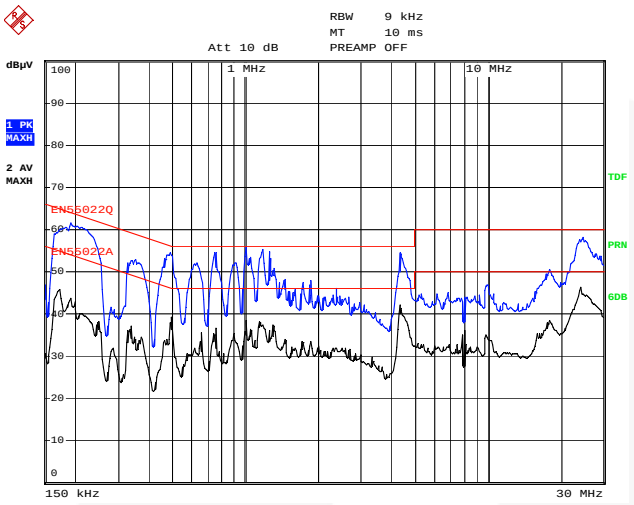


Figure 51. 115V$_{AC}$, Line

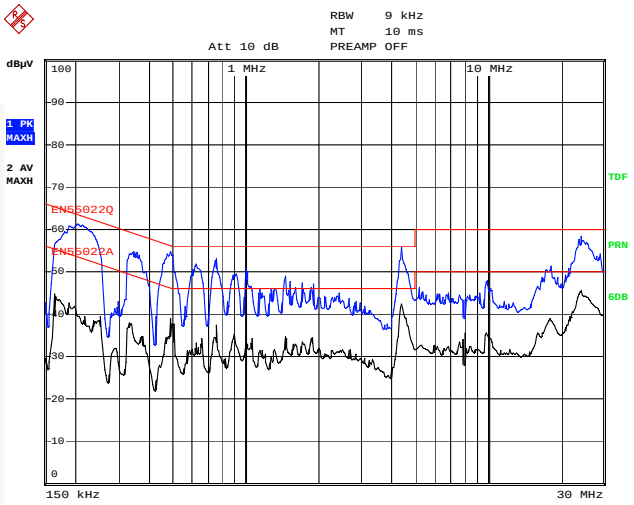


Figure 52. 115V$_{AC}$, Neutral

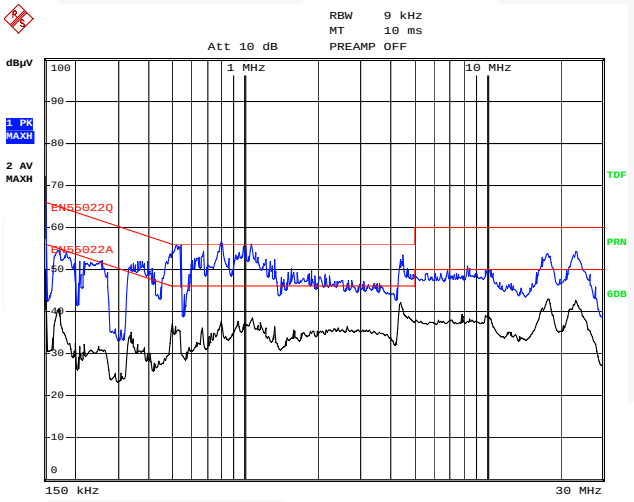


Figure 53. 230$_{VAC}$, Line

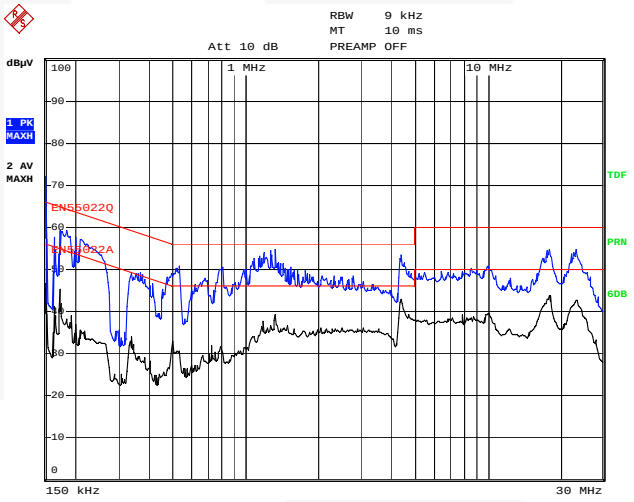


Figure 54. 230V$_{AC}$, Neutral

11. References

[1] *FAN9611 / FAN9612 — Interleaved Dual BCM PFC Controllers*

[2] *AN-6086 — Design Considerations for Interleaved Boundary-Conduction Mode PFC Using FAN9611 / FAN9612*

12. Ordering Information

Orderable Part Number	Description
FEBFAN9611_S01U300A	FAN9611 300W Evaluation Board

13. Revision History

Date	Revision	Description
February 2012	0.0.1	Initial release