# Product Specification

# 10km 100GBASE-LR4 CFP2 Optical Transceiver Module

# FTLC1122RDNL

## PRODUCT FEATURES

- Hot-pluggable CFP2 form factor
- Supports 103.1Gb/s aggregate bit rates
- Power dissipation < 5W
- RoHS-6 compliant (lead-free)
- Commercial case temperature range of 0°C to 75°C
- Single 3.3V power supply
- Maximum link length of 10km on Single Mode Fiber (SMF)
- 4x26Gb/s DFB-based LAN-WDM transmitter
- 4x26G electrical interface
- Duplex LC receptacles
- MDIO management interface

## APPLICATIONS

- 100GBASE-LR4 100G Ethernet

Finisar's 2nd generation, FTLC1122RDNL 100G CFP2 transceiver modules are designed for use in 100 Gigabit Ethernet interfaces over single mode fiber. They are compliant with the CFP MSA[1] and IEEE 802.3ba 100GBASE-LR4[2] specifications. Digital diagnostics functions are available via the MDIO interface, as specified by the CFP MSA and Finisar Application Note AN-2118[5]. The transceiver is RoHS compliant and lead-free per Directive 2011/65/EU[3], and Finisar Application Note AN-2038[4].

## PRODUCT SELECTION

**FTLC1122RDNL**

| | |
|---|---|
| R: | 100GE-LR4 maximum bit rate (103.1 Gb/s) |
| D: | 4x25G LAN-WDM optical architecture |
| N: | Flat top module (no heat sink) |
| L: | LC straight receptacles |

## I. Pin Descriptions

Per CFP MSA[1].

| | Top Row | | Bottom Row |
|---|---|---|---|
| 104 | GND | 1 | GND |
| 103 | N.C. | 2 | *{TX_MCLKn}* |
| 102 | N.C. | 3 | *{TX_MCLKp}* |
| 101 | GND | 4 | GND |
| 100 | TX3n | 5 | N.C. |
| 99 | TX3p | 6 | N.C. |
| 98 | GND | 7 | 3.3V_GND |
| 97 | TX2n | 8 | 3.3V_GND |
| 96 | TX2p | 9 | 3.3V |
| 95 | GND | 10 | 3.3V |
| 94 | N.C. | 11 | 3.3V |
| 93 | N.C. | 12 | 3.3V |
| 92 | GND | 13 | 3.3V_GND |
| 91 | N.C. | 14 | 3.3V_GND |
| 90 | N.C. | 15 | VND_IO_A |
| 89 | GND | 16 | VND_IO_B |
| 88 | TX1n | 17 | PRG_CNTL1 |
| 87 | TX1p | 18 | PRG_CNTL2 |
| 86 | GND | 19 | PRG_CNTL3 |
| 85 | TX0n | 20 | PRG_ALRM1 |
| 84 | TX0p | 21 | PRG_ALRM2 |
| 83 | GND | 22 | PRG_ALRM3 |
| 82 | N.C. | 23 | GND |
| 81 | N.C. | 24 | TX_DIS |
| 80 | GND | 25 | RX_LOS |
| 79 | *{REFCLKn}* | 26 | MOD_LOPWR |

| | Top Row | | Bottom Row |
|---|---|---|---|
| 78 | *{REFCLKp}* | 27 | MOD_ABS |
| 77 | GND | 28 | MOD_RSTn |
| 76 | N.C. | 29 | GLB_ALRMn |
| 75 | N.C. | 30 | GND |
| 74 | GND | 31 | MDC |
| 73 | RX3n | 32 | MDIO |
| 72 | RX3p | 33 | PRTADR0 |
| 71 | GND | 34 | PRTADR1 |
| 70 | RX2n | 35 | PRTADR2 |
| 69 | RX2p | 36 | VND_IO_C |
| 68 | GND | 37 | VND_IO_D |
| 67 | N.C. | 38 | VND_IO_E |
| 66 | N.C. | 39 | 3.3V_GND |
| 65 | GND | 40 | 3.3V_GND |
| 64 | N.C. | 41 | 3.3V |
| 63 | N.C. | 42 | 3.3V |
| 62 | GND | 43 | 3.3V |
| 61 | RX1n | 44 | 3.3V |
| 60 | RX1p | 45 | 3.3V_GND |
| 59 | GND | 46 | GND |
| 58 | RX0n | 47 | N.C. |
| 57 | RX0p | 48 | N.C. |
| 56 | GND | 49 | GND |
| 55 | N.C. | 50 | *{RX_MCLKn}* |
| 54 | N.C. | 51 | *{RX_MCLKp}* |
| 53 | GND | 52 | GND |

## Bottom Row Pin Descriptions

| PIN # | Name | I/O | Logic | Description |
|---|---|---|---|---|
| 1 | GND | | | |
| 2 | TX_MCLKn | | | **Supported.** |
| 3 | TX_MCLKp | | | **Supported.** |
| 4 | GND | | | |
| 5 | N.C. | | | |
| 6 | N.C. | | | |
| 7 | 3.3V_GND | | | **3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground** |
| 8 | 3.3V_GND | | | **3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground** |
| 9 | 3.3V | | | 3.3V Module Supply Voltage |
| 10 | 3.3V | | | 3.3V Module Supply Voltage |
| 11 | 3.3V | | | 3.3V Module Supply Voltage |
| 12 | 3.3V | | | 3.3V Module Supply Voltage |
| 13 | 3.3V_GND | | | **3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground** |
| 14 | 3.3V_GND | | | **3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground** |
| 15 | VND_IO_A | I/O | | Module Vendor I/O A. Do Not Connect! |
| 16 | VND_IO_B | I/O | | Module Vendor I/O B. Do Not Connect! |
| 17 | PRG_CNTL1 | I | LVCMOS w/ PUR | Programmable Control 1 set over MDIO |
| 18 | PRG_CNTL2 | I | LVCMOS w/ PUR | Programmable Control 2 set over MDIO |
| 19 | PRG_CNTL3 | I | LVCMOS w/ PUR | Programmable Control 3 set over MDIO |
| 20 | PRG_ALRM1 | O | LVCMOS | Programmable Alarm 1 set over MDIO |
| 21 | PRG_ALRM2 | O | LVCMOS | Programmable Alarm 2 set over MDIO |
| 22 | PRG_ALRM3 | O | LVCMOS | Programmable Alarm 3 set over MDIO |
| 23 | GND | | | |
| 24 | TX_DIS | I | LVCMOS w/ PUR | Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled |
| 25 | RX_LOS | O | LVCMOS | Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition |
| 26 | MOD_LOPWR | I | LVCMOS w/ PUR | Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled |
| 27 | MOD_ABS | O | GND | Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host |
| 28 | MOD_RSTn | I | LVCMOS w/ PDR | Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module |
| 29 | GLB_ALRMn | O | LVCMOS | Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host |
| 30 | GND | | | |
| 31 | MDC | I/O | 1.2V CMOS | Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba) |
| 32 | MDIO | I | 1.2V CMOS | Management Data Clock (electrical specs as per 802.3ae and ba) |
| 33 | PRTADR0 | I | 1.2V CMOS | MDIO Physical Port address bit 0 |
| 34 | PRTADR1 | I | 1.2V CMOS | MDIO Physical Port address bit 1 |
| 35 | PRTADR2 | I | 1.2V CMOS | MDIO Physical Port address bit 2 |
| 36 | VND_IO_C | I/O | | Module Vendor I/O C. Do Not Connect! |
| 37 | VND_IO_D | I/O | | Module Vendor I/O D. Do Not Connect! |
| 38 | VND_IO_E | I/O | | Module Vendor I/O E. Do Not Connect! |
| 39 | 3.3V_GND | | | **3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground** |
| 40 | 3.3V_GND | | | **3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground** |
| 41 | 3.3V | | | 3.3V Module Supply Voltage |
| 42 | 3.3V | | | 3.3V Module Supply Voltage |
| 43 | 3.3V | | | 3.3V Module Supply Voltage |
| 44 | 3.3V | | | 3.3V Module Supply Voltage |
| 45 | 3.3V_GND | | | **3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground** |
| 46 | GND | | | |
| 47 | N.C. | | | |
| 48 | N.C. | | | |
| 49 | GND | | | |
| 50 | RX_MCLKn | | | **Supported.** |
| 51 | RX_MCLKp | | | **Supported.** |
| 52 | GND | | | |

## II. Absolute Maximum Ratings

Module performance is not guaranteed beyond the operating range (see Section VI). Exceeding the limits below may damage the transceiver module permanently.

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| Maximum Supply Voltage | Vcc | -0.5 | | 4.0 | V | |
| Storage Temperature | $T_S$ | -40 | | 85 | °C | |
| Case Operating Temperature | $T_{OP}$ | 0 | | 75 | °C | |
| Relative Humidity | RH | 15 | | 85 | % | 1 |
| Receiver Damage Threshold, per Lane | $P_{Rdmg}$ | 5.5 | | | dBm | |

Notes:
1. Non-condensing.

## III. Electrical Characteristics (EOL, $T_{OP}$ = 0 to 75 °C, $V_{CC}$ = 3.2 to 3.4 Volts)

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| Supply Voltage | Vcc | 3.2 | | 3.4 | V | |
| Supply Current | Icc | | | 2.5 | A | |
| Module total power | P | | 4.5 | 5 | W | 1 |
| **Transmitter** | | | | | | |
| Signaling rate per lane | | | | 25.78 | Gb/s | 2 |
| Input differential impedance | $R_{in}$ | CAUI-4 as defined by IEEE P802.3bm | | | Ω | |
| Differential data input swing per lane | Vin,pp | | | | mV | |
| Data input rise time tolerance | $t_r$ | | | | ps | |
| Data input rise time tolerance | $t_f$ | | | | ps | |
| Electrical input eye mask definition | {X1, X2}<br>{Y1, Y2} | | | | UI<br>mV | |
| **Receiver** | | | | | | |
| Signaling rate per lane | | | | 25.78 | Gb/s | 2 |
| Differential data output swing per lane | Vout,pp | CAUI-4 as defined by IEEE P802.3bm | | | mV | |
| Data output rise time | $t_r$ | | | | ps | |
| Data output fall time | $t_f$ | | | | ps | |
| Electrical output eye mask definition | {X1, X2}<br>{Y1, Y2} | | | | UI<br>mV | |
| Power Supply Noise Tolerance | Vrip | Per Table 4-1 in the CFP2 MSA document[1] | | | | |

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. +/- 100ppm

### FTLC1122RDNL Clocking Signals

| Clock Name | Status | I/O | Value |
|---|---|---|---|
| REFCLK | Not Required | I | N/A (terminated internally) |
| TX_MCLK | Supported | O | 1/8 of network line rate |
| RX_MCLK | Supported | O | 1/8 of network line rate |

## IV. Optical Characteristics (EOL, $T_{OP}$ = 0 to 75°C, $V_{CC}$ = 3.2 to 3.4 Volts)

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Signaling Speed per Lane | | 25.78 | | 25.78 | Gb/s | 1 |
| Lane center wavelengths (range) | | 1294.53 – 1296.59<br>1299.02 – 1301.09<br>1303.54 – 1305.63<br>1308.09 – 1310.19 | | | nm | |
| Total Average Launch Power | $P_{OUT}$ | | | 10.5 | dBm | |
| Transmit OMA per Lane | TxOMA | -1.3 | | 4.5 | dBm | |
| Average Launch Power per Lane | $TXP_x$ | -4.3 | | 4.5 | dBm | 2 |
| Optical Extinction Ratio | ER | 4 | | | dB | |
| Sidemode Suppression ratio | $SSR_{min}$ | 30 | | | dB | |
| Transmitter Dispersion Penalty | TDP | | 0.3 | 2.2 | dB | |
| Average launch power of OFF transmitter, per lane | | | | -30 | dBm | |
| Relative Intensity Noise | RIN | | | -130 | dB/Hz | |
| Optical Return Loss Tolerance | | | | 20 | dB | |
| Transmitter Reflectance | | | | -12 | dB | |
| Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} | | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | |
| **Receiver** | | | | | | |
| Signaling Speed per Lane | | 25.78 | | 25.78 | GBd | 3 |
| Lane center wavelengths (range) | | 1294.53 – 1296.59<br>1299.02 – 1301.09<br>1303.54 – 1305.63<br>1308.09 – 1310.19 | | | nm | |
| Receive Power (OMA) per Lane | RxOMA | | | 4.5 | dBm | |
| Average Receive Power per Lane | $RXP_x$ | -10.6 | | 4.5 | dBm | 4 |
| Receiver Sensitivity (OMA) per Lane | Rxsens | | | -8.6 | dBm | |
| Stressed Receiver Sensitivity (OMA) per Lane | SRS | | | -6.8 | dBm | |
| Return Loss | RL | -26 | | | dB | |
| Vertical eye closure penalty, per lane | | | | 1.8 | dB | |
| Receive electrical 3 dB upper cutoff frequency, per lane | | | | 31 | GHz | |
| LOS De-Assert | $LOS_D$ | | | -11.6 | dBm | |
| LOS Assert | $LOS_A$ | | | -13.6 | dBm | |
| LOS Hysteresis | | | 1 | | dBm | |

Notes:
1. Transmitter consists of 4 lasers operating at 25.78Gb/s each.
2. Minimum value is informative.
3. Receiver consists of 4 photodetectors operating at 25.78Gb/s each.
4. Minimum value is informative, equals min TxOMA with infinite ER and max channel insertion loss.

## V. General Specifications

| Parameter | Symbol | Min | Typ | Max | Units | Ref. |
|---|---|---|---|---|---|---|
| Bit Rate (all wavelengths combined) | BR | | | 103.1 | Gb/s | 1 |
| Bit Error Ratio @25.78Gb/s | BER1 | | | $10^{-12}$ | | 2 |
| **Maximum Supported Distances** | | | | | | |
| Fiber Type | | | | | | |
| SMF per G.652 | Lmax1 | | | 10 | km | |

Notes:

1. Supports 100GBASE-LR4 per IEEE 802.3ba.
2. Tested with a $2^{31} - 1$ PRBS.

## VI. Environmental Specifications

Finisar FTLC1122 CFP2 transceivers have a commercial operating case temperature range of 0°C to +75°C.

| Parameter | Symbol | Min | Typ | Max | Units | Ref. |
|---|---|---|---|---|---|---|
| Case Operating Temperature | $T_{op}$ | 0 | | 75 | °C | |
| Storage Temperature | $T_{sto}$ | -40 | | 85 | °C | |

## VII. Regulatory Compliance

Finisar FTLC1122 CFP2 transceivers are Class 1 Laser Products. They are certified per the following standards:

| Feature | Agency | Standard | Certificate Number |
|---|---|---|---|
| Laser Eye Safety | FDA/CDRH | CDRH 21 CFR 1040 and Laser Notice 50 | 9210176 |
| | CSA | IEC60825-1:2014 | 70119867 |
| | TüV | EN60825-1: 2014<br>EN 60825-2: 2004+A1+A2 | R72130387 |
| Electrical Safety | CSA | IEC60950-1:2005+A1+A2, | 70119867 |
| | TüV | EN60950-1:2006+A11+A1+A12+A2 | R72130387 |
| | CSA | CAN/CSA-C22.2 no 60950-1-07+A1,<br>UL 60950-1-2011 | 2375840 |

Copies of the referenced certificates are available at Finisar Corporation upon request.

## VIII. Digital Diagnostics Functions

FTLC1122 CFP2 transceivers support the MDIO-based diagnostics interface specified in the CFP MSA[1]. See Finisar Application Note AN-2118.

## IX. Memory Contents

Per the CFP MSA[1]. See Finisar Application Note AN-2118.

## X. Host PCB Layout and Bezel Recommendations

Per CFP2 Hardware Specification[1].

## XI. Mechanical Specifications

Finisar FTLC1122 CFP2 transceivers are compatible with the CFP2 Hardware Specification for pluggable form factor modules.

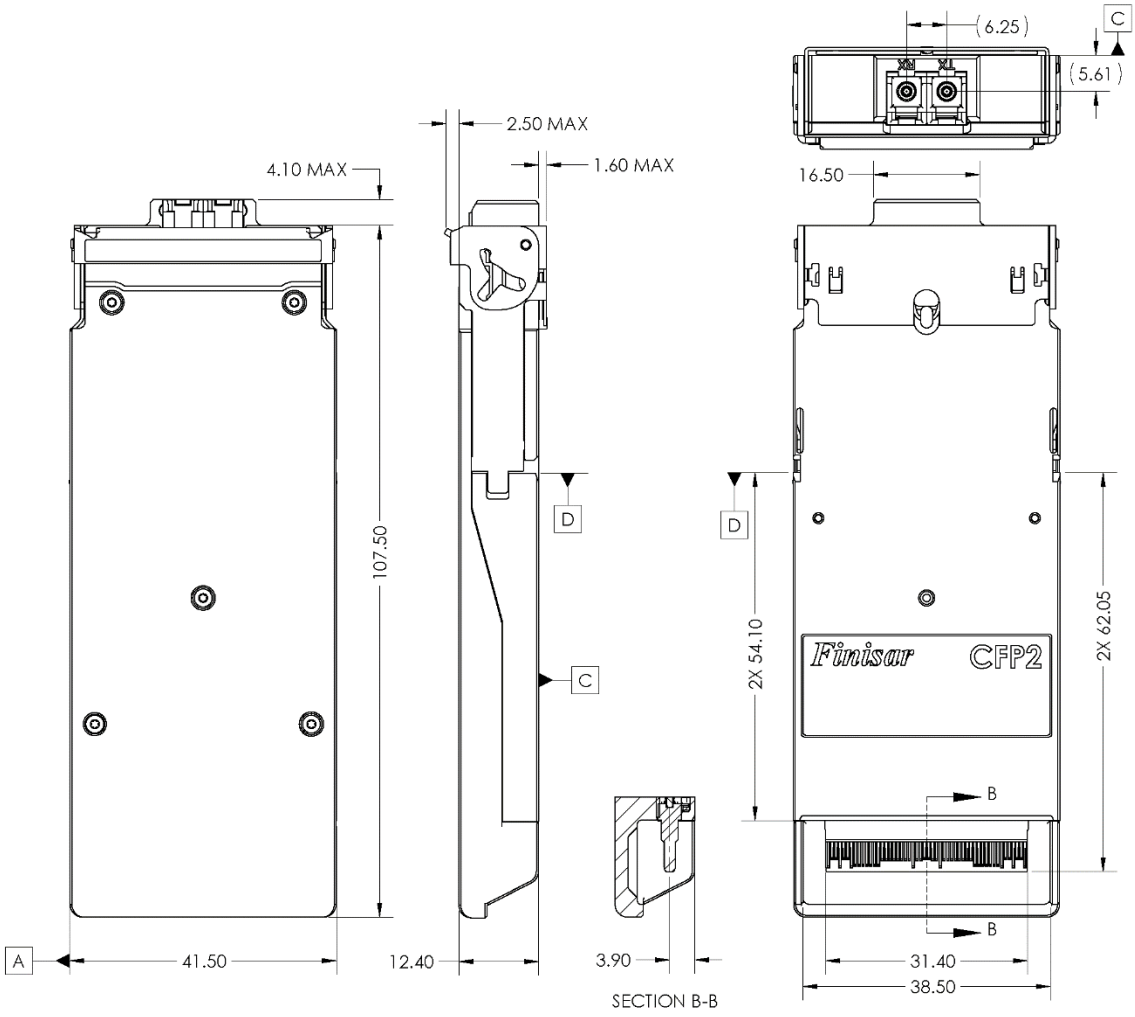


**Figure 1. FTLC1122RDNL Mechanical Dimensions.**


**Figure 2. Standard Product Label**

## XII. References

1. CFP2 Hardware Specification and CFP MSA Management Interface Specifications (MIS), Rev 2.4.; CFP MSA, www.cfp-msa.org

2. IEEE 802.3ba, PMD Type 100GBASE-LR4.

3. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," June 8, 2011.

4. "Application Note AN-2038: Finisar Implementation Of RoHS Compliant Transceivers", Finisar Corporation, January 21, 2005.

5. Application Note AN-2118, Finisar Corporation.

6. IEEE P802.3bm, CAUI-4 Interface.

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