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# LC79431KNE

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CMOS LSI

## Dot-Matrix LCD Drivers

### Overview

The LC79431KNE is a large-scale dot matrix LCD common driver LSI. The LC79431KNE contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC79431KNE can be used in conjunction with segment driver LC79401KNE (QIP100E) to drive a wide-screen LCD panel.

### Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- On-chip input/output pins support a further increases in bit number
- Supports externally supplied bias voltage
- Operating power supply voltage/operating temperature include
  - $V_{DD}$  (Logic section) : 2.7 to 5.5V/-20 to +85°C
  - $V_{DD-VEE}$  (LCD section) : 12 to 32V/-20 to +85°C
- CMOS process
- 100-pin flat plastic package (QIP100E)

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## Specifications

**Absolute Maximum Ratings** at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (Logic)	$V_{DD}$ max		-0.3 to +7.0	V
Maximum supply voltage (LCD)	$V_{DD}-V_{EE}$ max	*1	0 to 35	V
Maximum input voltage	$V_I$ max		-0.3 to $V_{DD}+0.3$	V
Storage temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

Note \*1 The following relations between elements should be maintained:  $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$ ,  $V_{DD}-V_2 \leq 7\text{V}$ ,  $V_5-V_{EE} \leq 7\text{V}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Allowable Operating Ranges** at  $T_a = -20$  to  $+85^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage (Logic)	$V_{DD}$		2.7		5.5	V
Supply voltage (LCD)	$V_{DD}-V_{EE}$	*2, 3	12		32	V
Input high level voltage	$V_{IH}$	DIO1, DIO80, CP, M, RS/LS, DISPOFF	$0.8V_{DD}$			V
Input low level voltage	$V_{IL}$	DIO1, DIO80, CP, M, RS/LS, DISPOFF			$0.2V_{DD}$	V
CP Shift clock	$f_{CP}$	CP			1	MHz
CP pulse width	$t_{WC}$	CP	63			ns
Setup time	$t_{SETUP}$	DIO1 $\rightarrow$ CP, DIO80 $\rightarrow$ CP	100			ns
Hold time	$t_{HOLD}$	DIO1 $\rightarrow$ CP, DIO80 $\rightarrow$ CP	100			ns
CP rise time	$t_R$	CP			50	ns
CP fall time	$t_F$	CP			50	ns

Note \*2 The following relations between elements should be maintained:  $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$ ,  $V_{DD}-V_2 \leq 7\text{V}$ ,  $V_5-V_{EE} \leq 7\text{V}$

\*3 When the power supply is turned on, power to the LCD driver is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

**Electrical Characteristics** at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Input high level current	$I_{IH}$	$V_{IN}=V_{DD}$ , $V_{DD}=5.5\text{V}$ , DIO1, DIO80, CP, M, RS/LS, DISPOFF			1	$\mu\text{A}$
Input low level current	$I_{IL}$	$V_{IN}=V_{SS}$ , $V_{DD}=5.5\text{V}$ , DIO1, DIO80, CP, M, RS/LS, DISPOFF	-1			$\mu\text{A}$
Output high level voltage	$V_{OH}$	$I_{OH}=-0.4\text{mA}$ , DIO1, DIO80	$V_{DD}-0.4$			V
Output low level voltage	$V_{OL}$	$I_{OL}=0.4\text{mA}$ , DIO1, DIO80			0.4	V
Driver on resistance	$R_{ON(1)}$	$V_{DD}-V_{EE}=30\text{V}$ , $ V_{DE}-V_{OL} =0.5\text{V}$ $V_{DD}=4.5\text{V}$ , O1 to O80 *4			1.0	$\text{k}\Omega$
	$R_{ON(2)}$	$V_{DD}-V_{EE}=20\text{V}$ , $ V_{DE}-V_{OL} =0.5\text{V}$ $V_{DD}=4.5\text{V}$ , O1 to O80 *4			1.0	$\text{k}\Omega$
Consumable current drain (1)	$I_{SS}$	$V_{DD}-V_{EE}=30\text{V}$ , CP=14kHz no-load, $V_{DD}=5.5\text{V}$ ; $V_{SS}$			100	$\mu\text{A}$
Consumable current drain (2)	$I_{EE}$	$V_{DD}-V_{EE}=30\text{V}$ , CP=14kHz no-load, $V_{DD}=5.5\text{V}$ ; $V_{EE}$			100	$\mu\text{A}$
Input capacitance	$C_I$	$f=1\text{MHz}$ ; CP		6		$\text{pF}$

Note \*4  $V_{DE} = V_1$  or  $V_2$  or  $V_5$  or  $V_{EE}$ ,  $V_1 = V_{DD}$ ,  $V_2 = 16/17 (V_{DD}-V_{EE})$ ,  $V_5 = 1/17 (V_{DD}-V_{EE})$

**Switching Characteristics** at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{DD} = 2.7$  to  $5.5\text{V}$

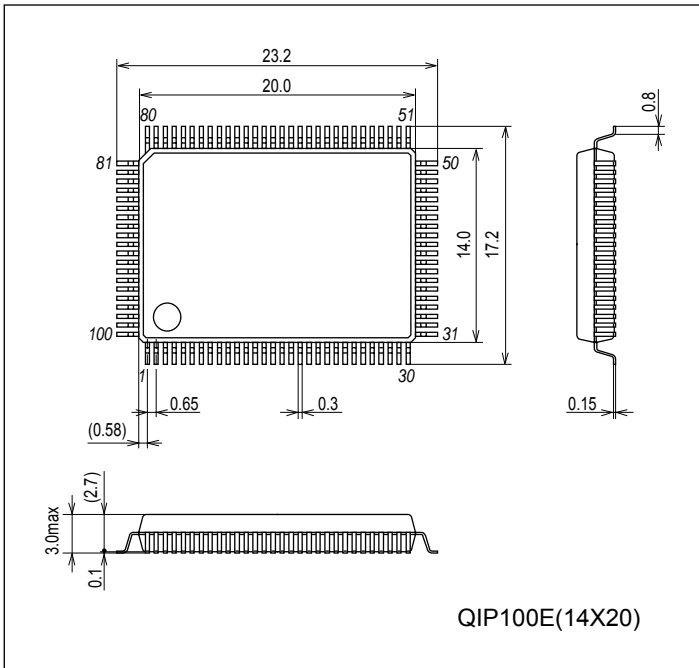
Parameter	Symbol	Conditions	min	typ	max	unit
Output delay time	$t_{PLH}$	$C_L=15\text{pF}$ ; CP $\rightarrow$ DIO1, CP $\rightarrow$ DIO80			250	ns
	$t_{PHL}$	$C_L=15\text{pF}$ ; CP $\rightarrow$ DIO1, CP $\rightarrow$ DIO80			250	ns

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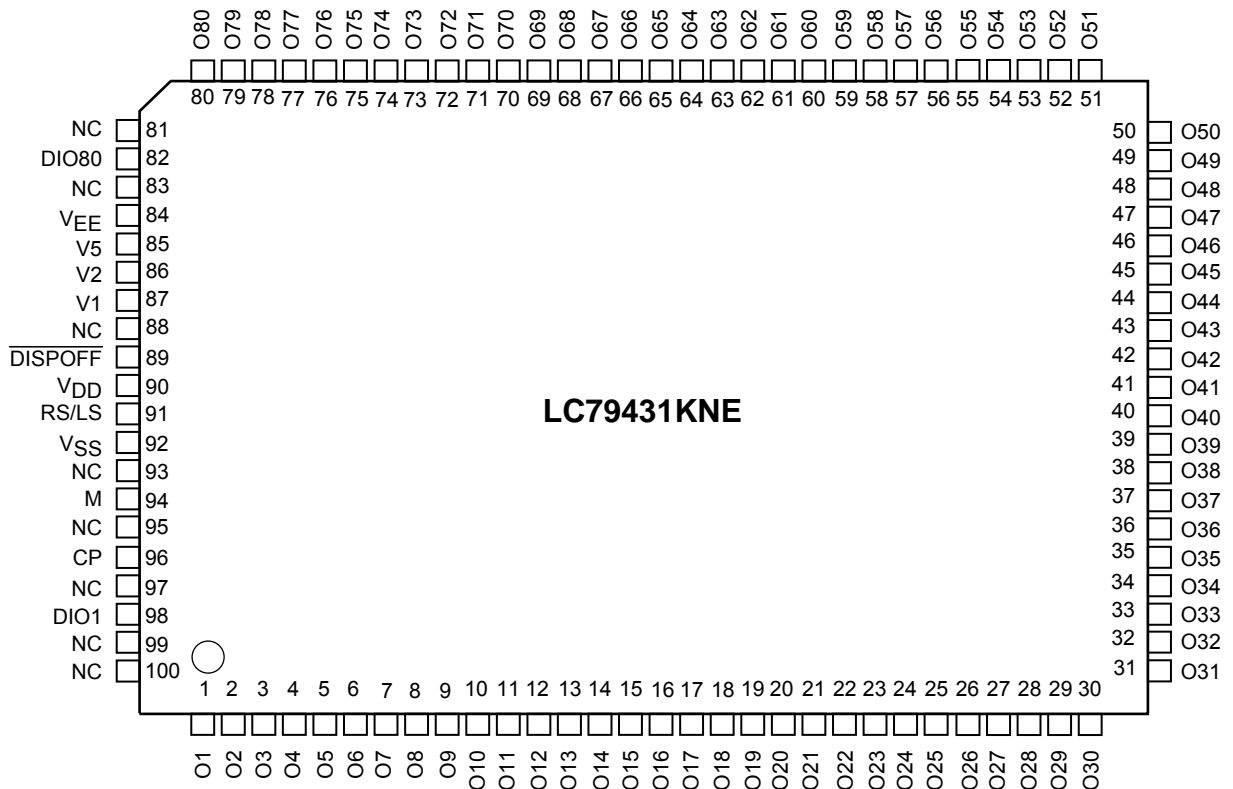
## Package Dimensions

unit:mm (typ)

3151A



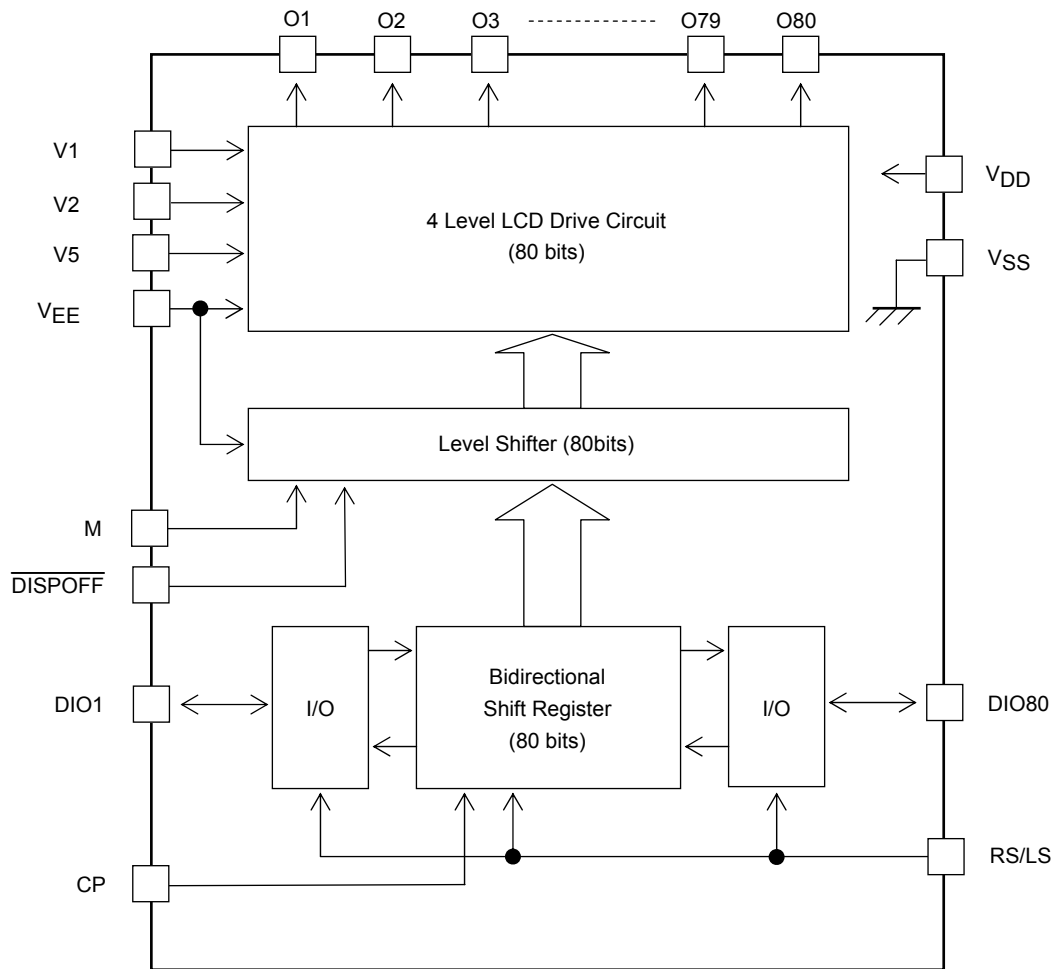
## Pin Assignment



Top view

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## Equivalent Circuit Block Diagram



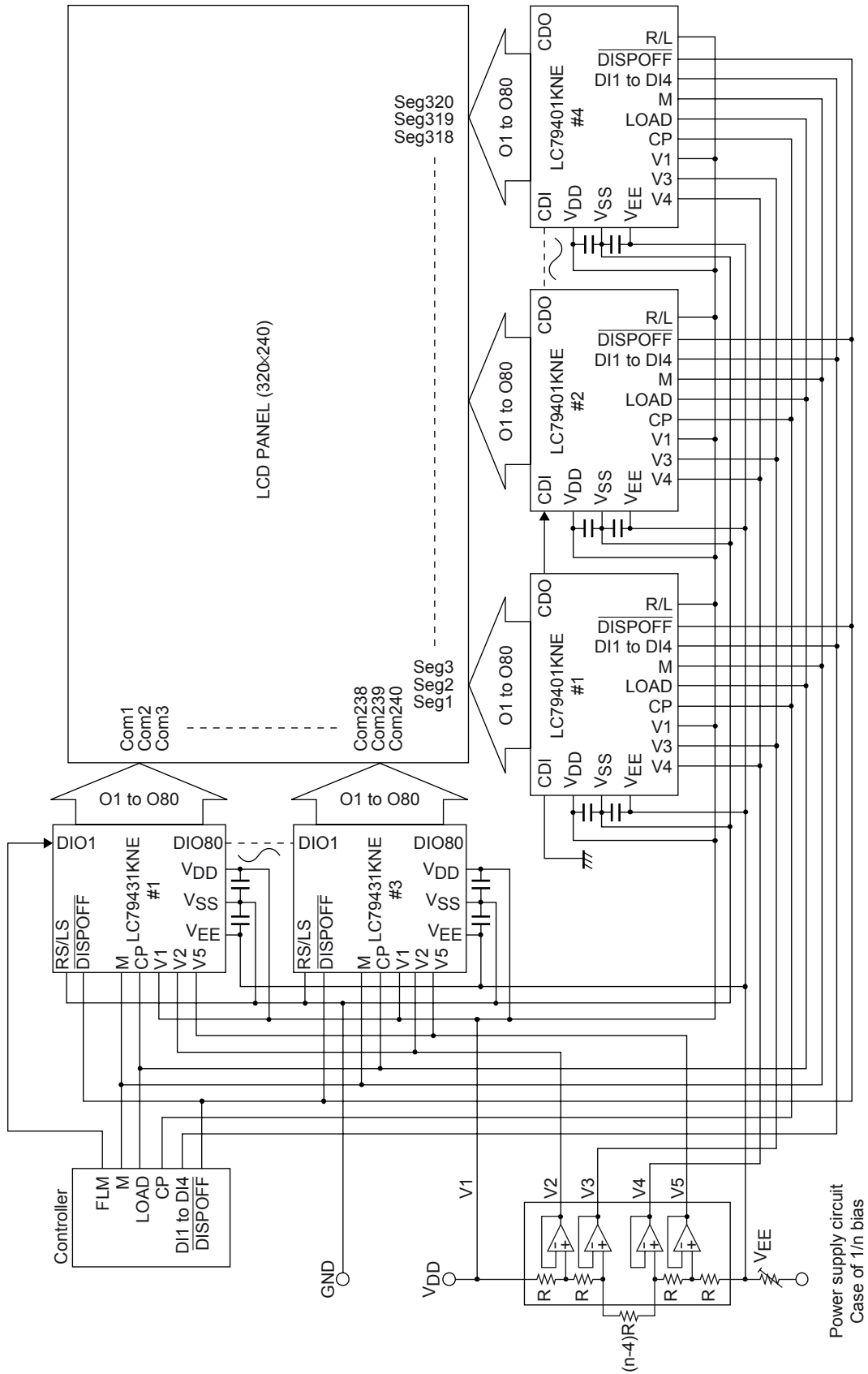
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## Pin Function

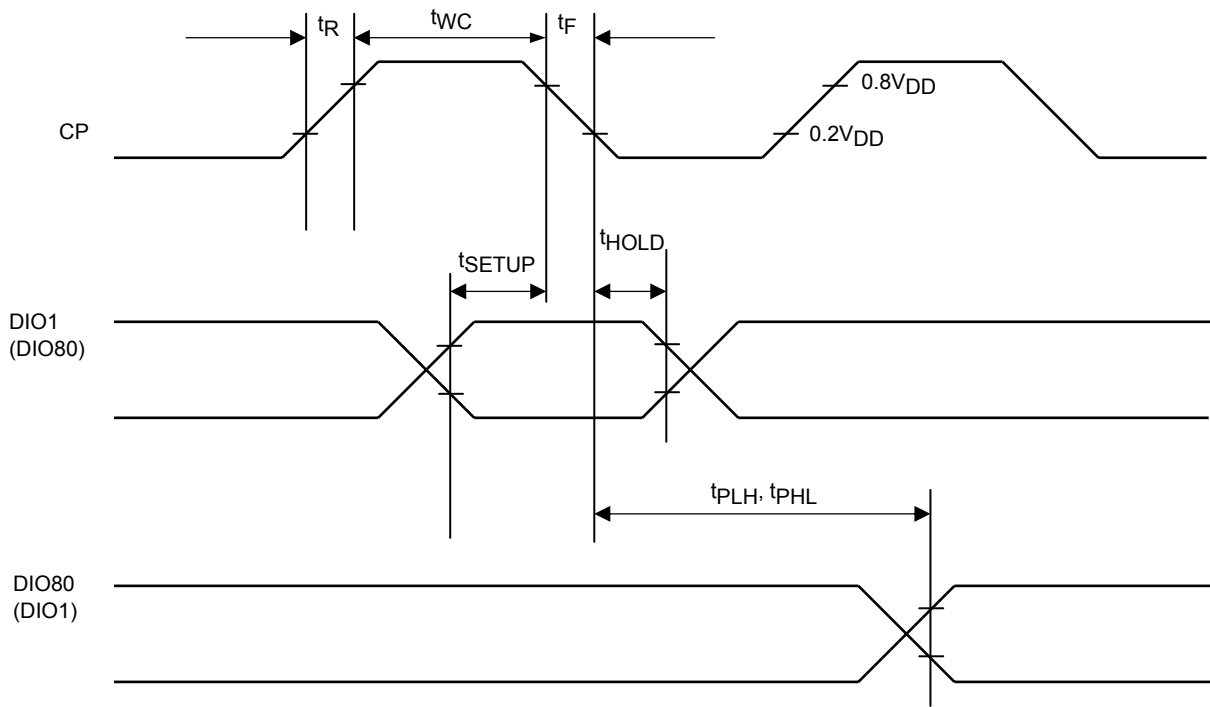
Pin No	Symbol	I/O	Function																								
90	V <sub>DD</sub>	Supply	V <sub>DD</sub> -V <sub>SS</sub> : Logic power supply V <sub>DD</sub> -V <sub>EE</sub> : LCD drive circuit power supply																								
92	V <sub>SS</sub>																										
84	V <sub>EE</sub>																										
87	V1	Supply	LCD drive level power supply V1, V <sub>EE</sub> : Selected level V2, V5 : Unselected level																								
86	V2																										
85	V5																										
96	CP	I	Bidirectional shift register shift clock (falling edge trigger)																								
98	DIO1	I/O	<table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 5px;"> <thead> <tr> <th style="width: 15%;">RS/LS</th> <th style="width: 40%;">Data Transfer Direction</th> <th style="width: 15%;">DIO1</th> <th style="width: 30%;">DIO80</th> </tr> </thead> <tbody> <tr> <td>L (Shift right)</td> <td>O1 → O80</td> <td>IN</td> <td>OUT</td> </tr> <tr> <td>H (Shift left)</td> <td>O80 → O1</td> <td>OUT</td> <td>IN</td> </tr> </tbody> </table>	RS/LS	Data Transfer Direction	DIO1	DIO80	L (Shift right)	O1 → O80	IN	OUT	H (Shift left)	O80 → O1	OUT	IN												
RS/LS	Data Transfer Direction	DIO1		DIO80																							
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82	DIO80	I/O																									
91	RS/LS	I																									
94	M	I	LCD drive output alternation signal																								
89	$\overline{\text{DISPOFF}}$	I	O1 to O80 output controlling input pins.																								
1 ⋮ 80	O1 ⋮ O80	O	<p>LCD drive outputs</p> <p>The output levels are determined by the combination of the output the data, The M signal, and the <math>\overline{\text{DISPOFF}}</math> pin as shown in the table.</p> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 5px;"> <thead> <tr> <th style="width: 15%;">M</th> <th style="width: 20%;">Data</th> <th style="width: 20%;"><math>\overline{\text{DISPOFF}}</math></th> <th style="width: 45%;">Output</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> <td>V2</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>V<sub>EE</sub></td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>V5</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>V1</td> </tr> <tr> <td>*</td> <td>*</td> <td>L</td> <td>V1</td> </tr> </tbody> </table> <p>* Don't care (May be set to either "H" or "L")</p>	M	Data	$\overline{\text{DISPOFF}}$	Output	L	L	H	V2	L	H	H	V <sub>EE</sub>	H	L	H	V5	H	H	H	V1	*	*	L	V1
M	Data	$\overline{\text{DISPOFF}}$	Output																								
L	L	H	V2																								
L	H	H	V <sub>EE</sub>																								
H	L	H	V5																								
H	H	H	V1																								
*	*	L	V1																								
81	NC	-	Must be left open.																								
83																											
88																											
93																											
95																											
97																											
99																											
100																											

# LC79431KNE

## Application Example (LC79401KNE/LC79431KNE)



Switching Characteristics Diagram



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