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Routing Guideline Views .bdl

1.0 SCOPE

This specification covers the high-speed PCB routing recommendations for the 0.80mm centerline Stacked zQSFP+ Connector series products listed below. The connector is a stacked dual port assembly and is available in a 2x1,2x2, 2X3 configuration. Eight differential pairs are assigned per port. The connector has 38 contacts per port of which 26 can be assigned to signals and 12 are for ground terminals. The connector is a right angle press-fit compliant pin type designed for use with 0.37mm finished vias for the signal pins.

The connector has compliant pin contacts for mechanical retention to the PC board. The connector provides inner electromagnetic interference (EMI) suppression ground spring-fingers that contact the mating plug and is available with either an outer Elastomeric or Metal EMI gasket that contacts the panel. The connector assembly is designed to be inserted through a standard bezel after being seated onto the PC board.

Disclaimer: *Molex does not guarantee the performance of the final product to match the information provided in this document. All information in this report is considered proprietary, confidential and the property of Molex Inc. This guide is not intended as a substitute for engineering analysis.*

Product Series	Description
171208-****	2X1 Connector with Elastomeric EMI Gasket
171262-****	2X3 Connector with Elastomeric EMI Gasket
171565-****	2X1 thru 2X3 Connector with Elastomeric EMI Gasket and Enhanced EMI cage
171722-****	2X1 thru 2X3 Connector with Metal EMI Gasket and Enhanced EMI cage
170879-****	2X1 Connector with Thermal Management Component
171233-****	2X3 Connector with Thermal Management Component

2.0 PC BOARD REQUIREMENTS

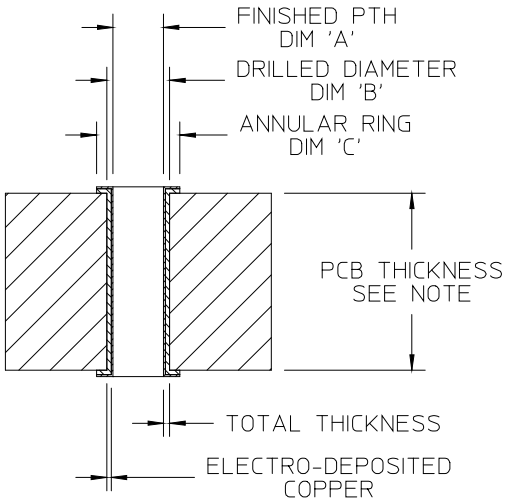
2.1 MATERIAL THICKNESS
The recommended minimum pc board thickness shall be 1.57 mm. Suitable pc board material shall be glass epoxy (FR-4 or G-10).

2.2 TOLERANCE
Maximum allowable bow of the pc board shall be 0.08 mm over the length of the connector assembly.

2.3 HOLE DIMENSIONS
The holes for the connector assembly must be drilled and plated through to dimensions specified in Figure 2.

2.4 LAYOUT
The holes for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Recommended hole pattern, dimensions, and tolerances are provided in Figure 3.

Recommended Hole Dimensions



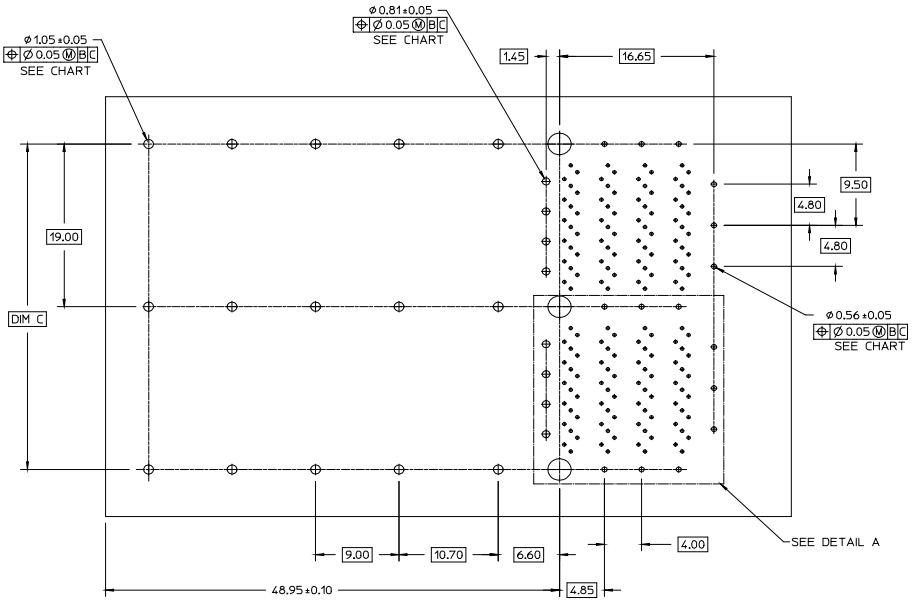
DIM. "A" MM / (INCH)	**DIM. "B"** MM / (INCH) - # DRILL	**DIM. "C"** MM / (INCH)
1.05+/-0.05 (.0413+/-.002)	1.181 (.0465) - # 56	1.40 (.055)
0.81+/-0.05 (.032+/-.002)	0.914 (.036) - # 64	1.16 (.046)
0.56+/-0.05 (.022+/-.002)	0.660 (.026) - # 71	0.91 (.036)
0.46+/-0.05 (.0181+/-.002)	0.572 (.022) - # 74	0.81 (.032)
0.37+/-0.05 (.0146+/-.002)	0.457 (.018) - # 77	0.72 (.028)

Note: Refer to appropriate sales drawing for recommended pcb holes and pcb thickness.

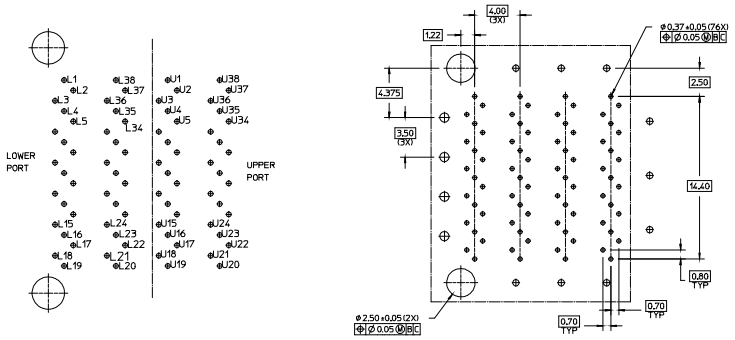
PLATING DETAIL FOR COMPLIANT PIN HOLES
Figure 2

Recommended PC Board Layout for the Connector Assembly

Connector



PORT SIZE	DIM C	1.05ø QUANTITY	0.56ø QUANTITY	0.81ø QUANTITY
2X1	19.00	10	9	4
2X2	38.00	15	15	8
2X3	57.00	20	21	12



Pattern Detail

Figure 3

REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
2	EC No: **UCP2013-5477** DATE: **2013/06/19**	**SI ROUTING GUIDELINES FOR ZQSFP+ STACKED CONNECTORS**	**4** of **13**

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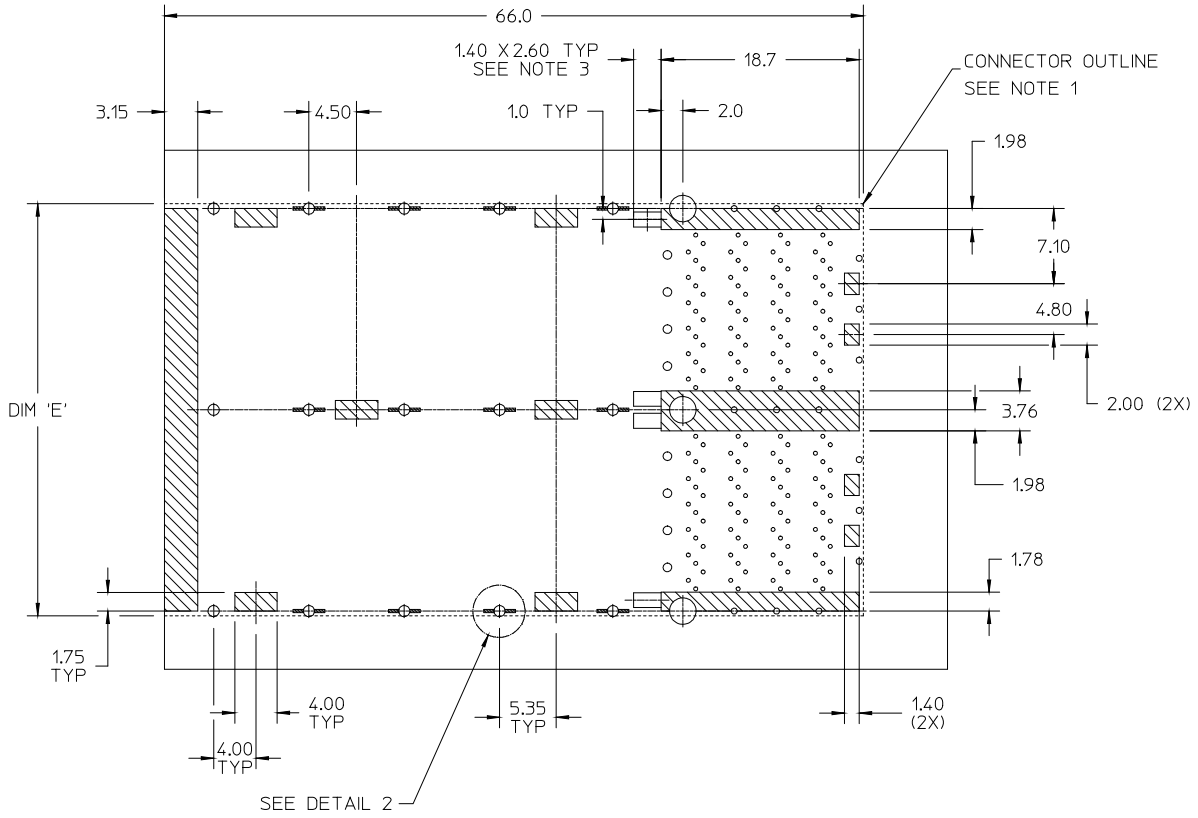
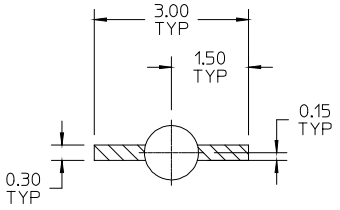
AS-171565-0002	**Jkachlic**		

Recommended Keep-out Zone Area Layout on PC Board for Connector Assembly



PORT SIZE	DIM E
2X1	19.5
2X2	38.5
2X3	57.5

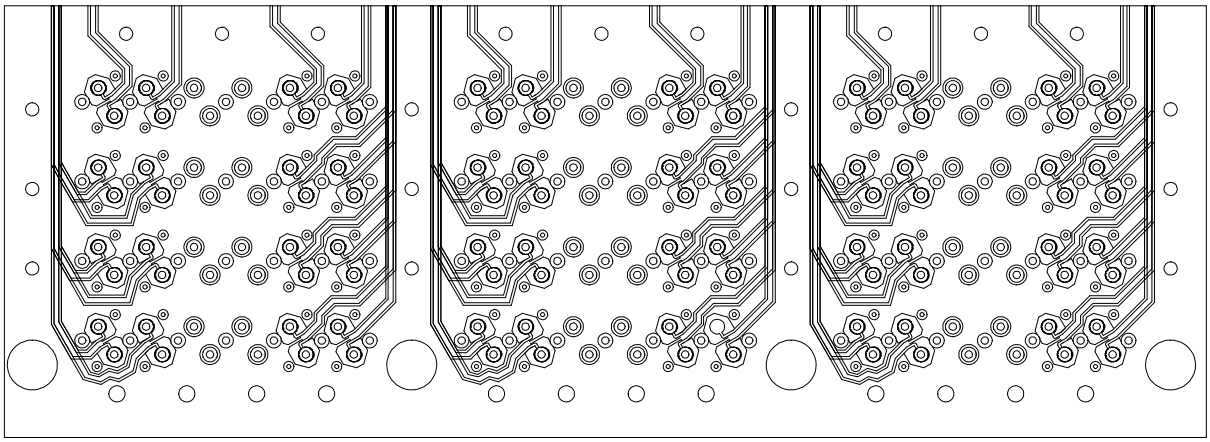


Notes:

1. The entire area under the connector cage is a component keep-out zone. The area under the connector module is a trace keep-out area
2. Cross hatched areas indicate places where the plastic housing and metal cage may be in contact with the PCB surface. These areas are trace keep-out zones.
3. These rectangular zones are for LED placement. LED height should not exceed 0.8 and placement should be centered within this LED keep-in zone.
4. Recommended LED chip package size is 0805.

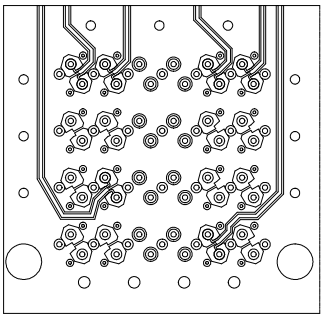
3.0 HIGH-SPEED ROUTING

3.1 GENERAL 2X3 ROUTING EXAMPLE

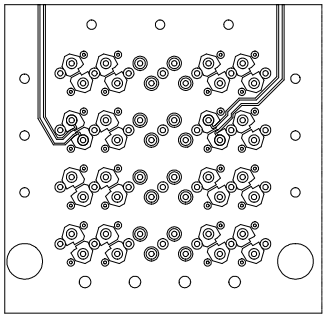


Showing 6 layers overlaid for a 2X3 side by side configuration with EMI pin field
Routing example shown for reference only.

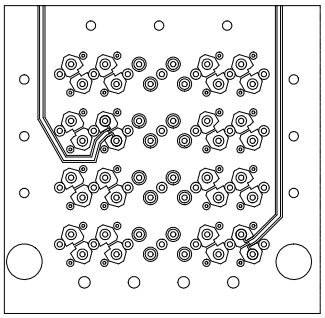
Shown with 0.127mm (0.005”) traces and 0.254mm (0.010”) spaces
0.75mm (0.0295”) spaces between pair traces.



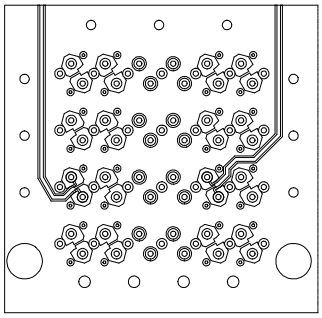
1ST LAYER



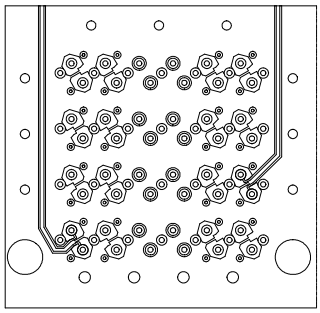
2ND LAYER



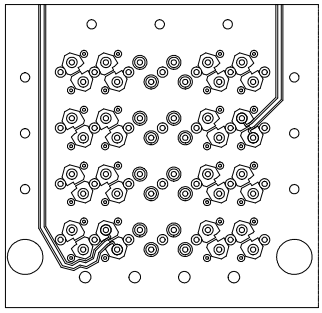
3RD LAYER



4TH LAYER



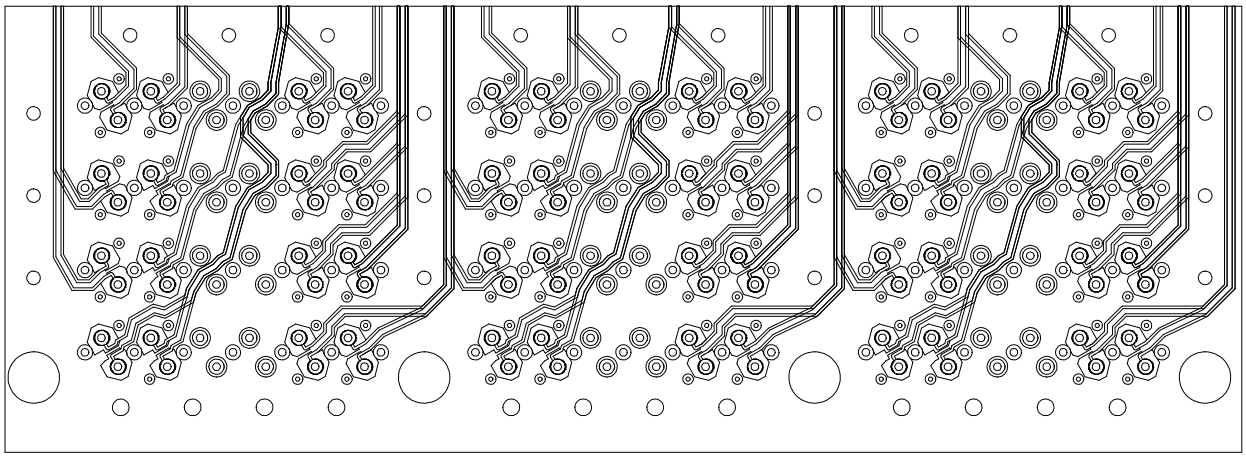
5TH LAYER



6TH LAYER

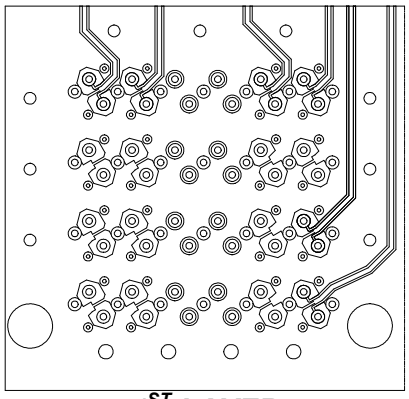
ZQSFP+ STACKED CONNECTOR

BOARD ROUTING RECOMMENDATIONS

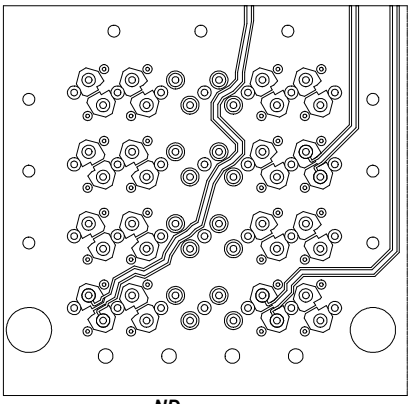


Showing 4 layers overlaid for a 2X3 side by side configuration with EMI pin field
Routing example shown for reference only.

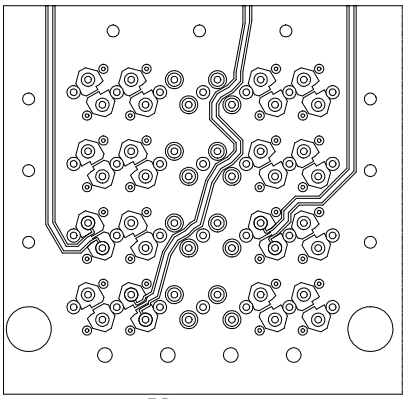
Shown with 0.127mm (0.005”) traces and 0.254mm (0.010”) spaces
0.75mm (0.0295”) spaces between pair traces.



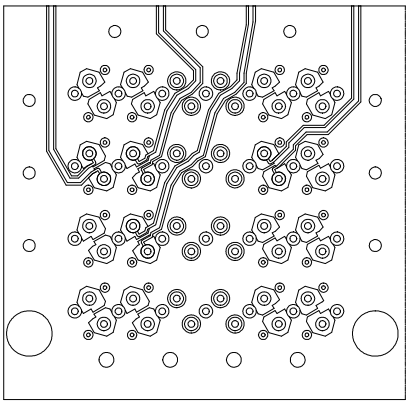
1ST LAYER



2ND LAYER



3RD LAYER



4TH LAYER

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2	EC No: **UCP2013-5477** DATE: **2013/06/19**	**SI ROUTING GUIDELINES FOR ZQSFP+ STACKED CONNECTORS**	**7** of **13**

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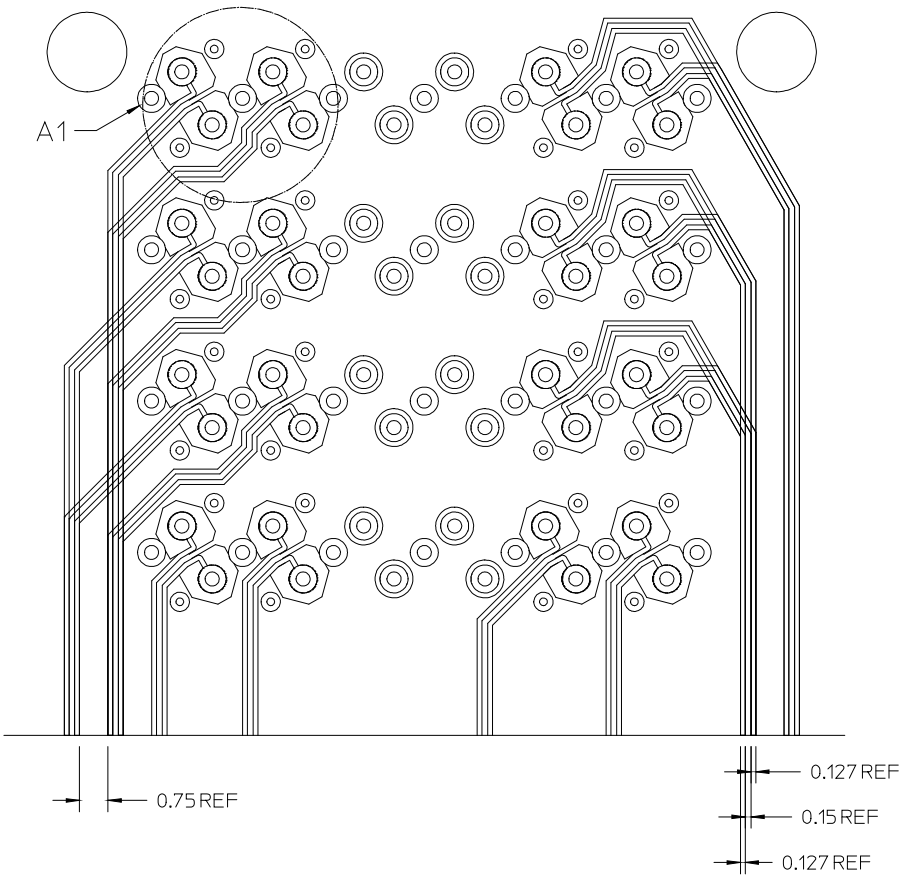
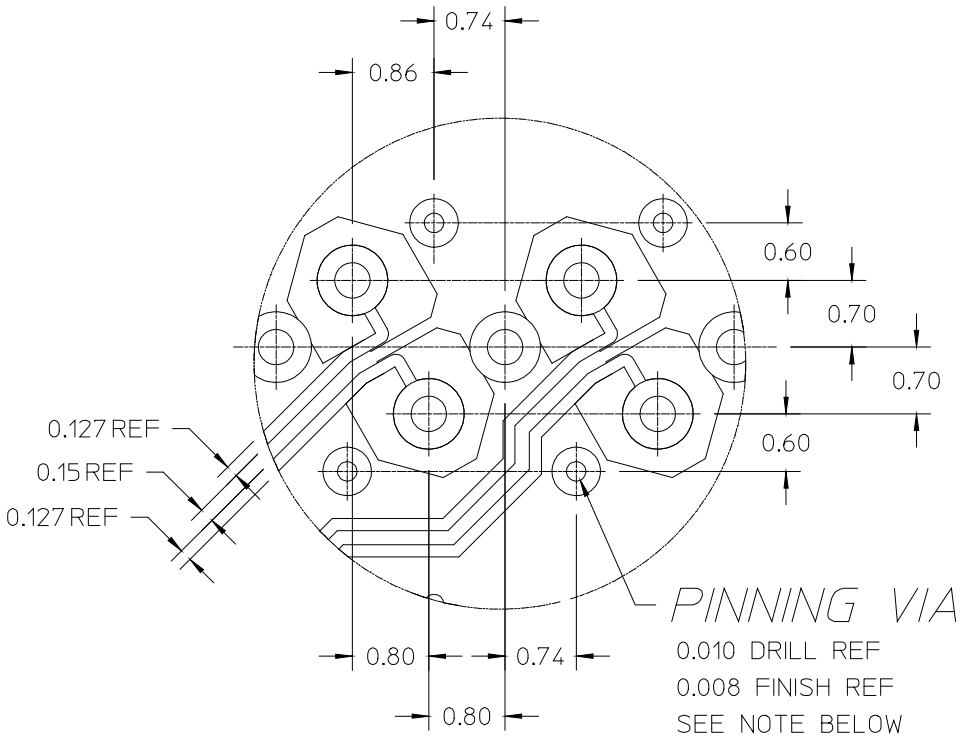
AS-171565-0002	**Jkachlic**		

3.2 HIGH-SPEED TRANSMISSION LINE PLANE



Reference ground layer shown and spacing between trace pairs
Routing example shown for reference only

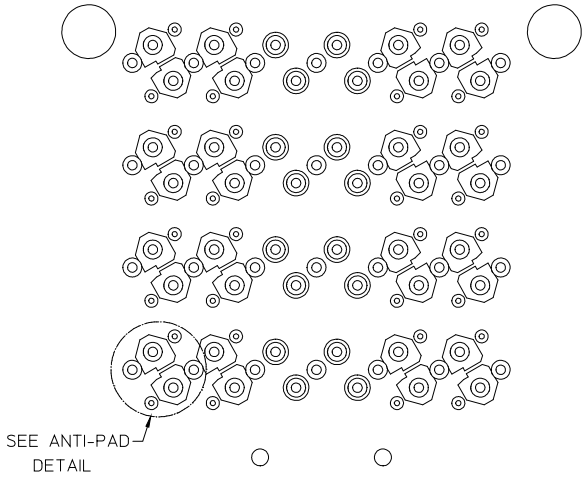


Trace detail typical for all trace positions

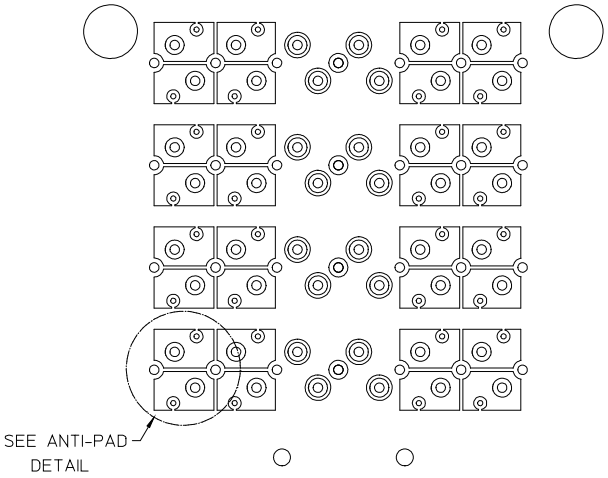
Note:
Option pinning VIA within connector footprint for additional electrical performance, location and size can vary from recommendation to meet board thickness, routing and electrical performance requirements.

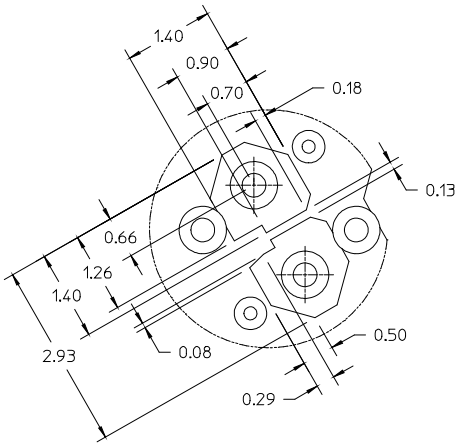
3.3 HIGH-SPEED REFERENCE PLANE ANTI-PAD

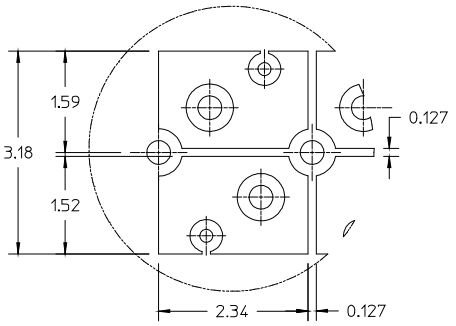
Signal Ground Planes



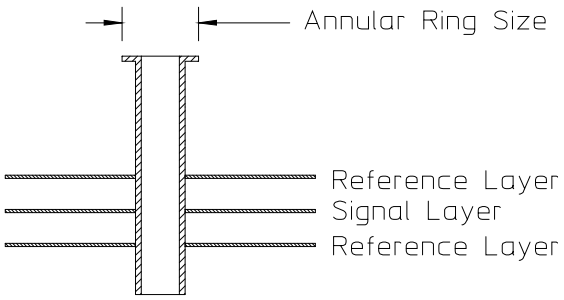
Non-Signal Planes



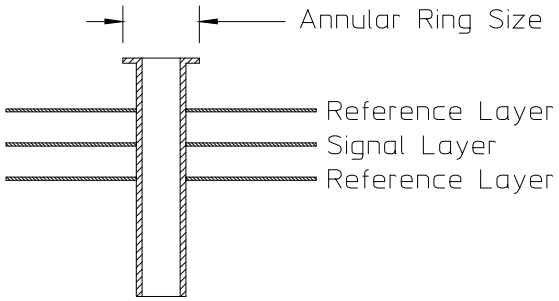




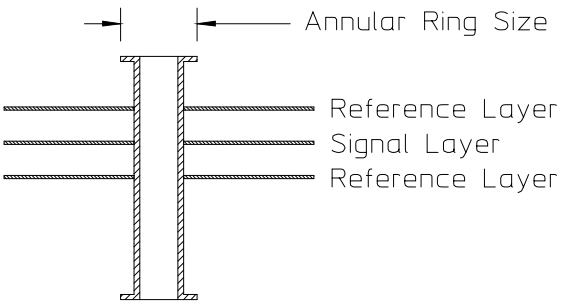
3.4 CONNECTOR PRESS-FIT INTERFACE VIA STUBS



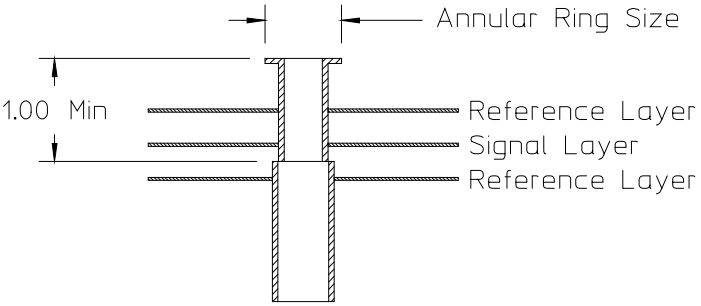
BOTTOM LAUNCH
DRIVEN VIA
(PREFERRED)



TOP LAUNCH
STUB VIA
(WORSE CASE)



STANDARD VIA CONFIGURATION



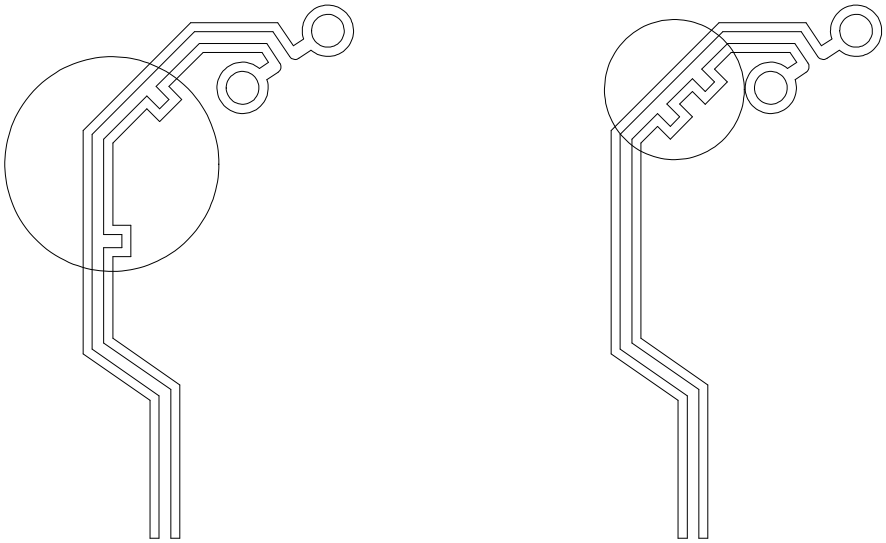
BACK DRILL DEPTH NOT TO EXCEED
1.00mm FROM TOP

Only two annular rings are required for retention of the press-fit via within the printed circuit consequently annular rings on the bottom layer are not needed. Removing the bottom layer annular ring helps minimize the parasitic stub capacitance created by the via.

The anti-pad can be used on other ground layers not shown above. Alternatively, the anti-pad can be made larger with a broader keep-out region on these other ground layers to minimize parasitic capacitance.

For the connector press-fit vias, specify not only the 0.37mm (0.014") finished hole size but also the 0.45715mm (0.018") drill size for the board fabrication.

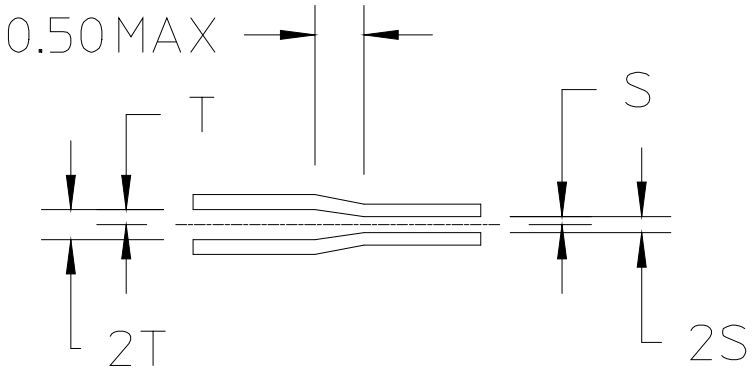
3.5 SKEW COMPENSATION



PREFERRED **NOT RECOMMENDED**

It is recommended that skew compensation be distributed verses grouped in one or more locations.

3.6 TRACE COMPARISON



TRANSITION SHOULD BE SYMETRIC

4.0 Pin Assignments

Notes:

1. See sheet no. 4 for physical locations of pin assignments
2. Reference SFF-8436 for further details

Lower Port

Pin	Symbol	Description
L1	GND	Ground
L2	Tx2n	Transmitter Inverted Data Input
L3	Tx2p	Transmitter Non-Inverted Data Input
L4	GND	Ground
L5	Tx4n	Transmitter Inverted Data Input
L6	Tx4p	Transmitter Non-Inverted Data Input
L7	GND	Ground
L8	ModSelL	Module Select
L9	ResetL	Module Reset
L10	Vcc Rx	+3.3V Power Supply Receiver
L11	SCL	2-wire serial interface clock
L12	SDA	2-wire serial interface data
L13	GND	Ground
L14	Rx3p	Receiver Non-Inverted Data Input
L15	Rx3n	Receiver Inverted Data Input
L16	GND	Ground
L17	Rx1p	Receiver Non-Inverted Data Input
L18	RX1n	Receiver Inverted Data Input
L19	GND	Ground

Pin	Symbol	Description
L38	GND	Ground
L37	Tx1n	Transmitter Inverted Data Input
L36	Tx1p	Transmitter Non-Inverted Data Input
L35	GND	Ground
L34	Tx3n	Transmitter Inverted Data Input
L33	Tx3p	Transmitter Non-Inverted Data Input
L32	GND	Ground
L31	LPMode	Low Power Mode
L30	Vcc1	+3.3V Power Supply
L29	Vcc Tx	+3.3V Power Supply Transmitter
L28	IntL	Interrupt
L27	ModPrsL	Module Present
L26	GND	Ground
L25	Rx4p	Receiver Non-Inverted Data Input
L24	Rx4n	Receiver Inverted Data Input
L23	GND	Ground
L22	Rx2p	Receiver Non-Inverted Data Input
L21	RX2n	Receiver Inverted Data Input
L20	GND	Ground

Upper Port

Pin	Symbol	Description
U1	GND	Ground
U2	Tx2n	Transmitter Inverted Data Input
U3	Tx2p	Transmitter Non-Inverted Data Input
U4	GND	Ground
U5	Tx4n	Transmitter Inverted Data Input
U6	Tx4p	Transmitter Non-Inverted Data Input
U7	GND	Ground
U8	ModSelL	Module Select
U9	ResetL	Module Reset
U10	Vcc Rx	+3.3V Power Supply Receiver
U11	SCL	2-wire serial interface clock
U12	SDA	2-wire serial interface data
U13	GND	Ground
U14	Rx3p	Receiver Non-Inverted Data Input
U15	Rx3n	Receiver Inverted Data Input
U16	GND	Ground
U17	Rx1p	Receiver Non-Inverted Data Input
U18	RX1n	Receiver Inverted Data Input
U19	GND	Ground

Pin	Symbol	Description
U38	GND	Ground
U37	Tx1n	Transmitter Inverted Data Input
U36	Tx1p	Transmitter Non-Inverted Data Input
U35	GND	Ground
U34	Tx3n	Transmitter Inverted Data Input
U33	Tx3p	Transmitter Non-Inverted Data Input
U32	GND	Ground
U31	LPMode	Low Power Mode
U30	Vcc1	+3.3V Power Supply
U29	Vcc Tx	+3.3V Power Supply Transmitter
U28	IntL	Interrupt
U27	ModPrsL	Module Present
U26	GND	Ground
U25	Rx4p	Receiver Non-Inverted Data Input
U24	Rx4n	Receiver Inverted Data Input
U23	GND	Ground
U22	Rx2p	Receiver Non-Inverted Data Input
U21	RX2n	Receiver Inverted Data Input
U20	GND	Ground

Cage

Pin	Symbol	Description
C1	GND	Ground
C2	GND	Ground
C3	GND	Ground
C4	GND	Ground
C5	GND	Ground
C6	GND	Ground
C7	GND	Ground

Pin	Symbol	Description
C8	GND	Ground
C9	GND	Ground
C10	GND	Ground
C11	GND	Ground
C12	GND	Ground
C13	GND	Ground